DATA SHEET

XA-SCC
CMOS 16-bit communications microcontroller

Preliminary specification

1999 Feb 23

IC25 Data Handbook

Philips Semiconductors

PHILIPS

GENERAL DESCRIPTION

The XA-SCC device is a member of Philips' XA (eXtended Architecture) family of high performance 16-bit single-chip microcontrollers.

The XA-SCC includes a complete onboard DRAM controller capable of supporting up to 32MegaBytes of DRAM.

The XA-SCC device combines many powerful communications oriented peripherals on one chip. 4 Full Function SCC's, 8 DMA channels (2 per SCC), hardware autobaud up to 921.6Kbps, IDL TDM interface, two timers/counters, 1 watchdog timer, and multiple general purpose I/O ports. It is suited for many high performance embedded communications functions, including ISDN terminal adaptors and Asynchronous Muxes.

SPECIFIC FEATURES OF THE XA-SCC

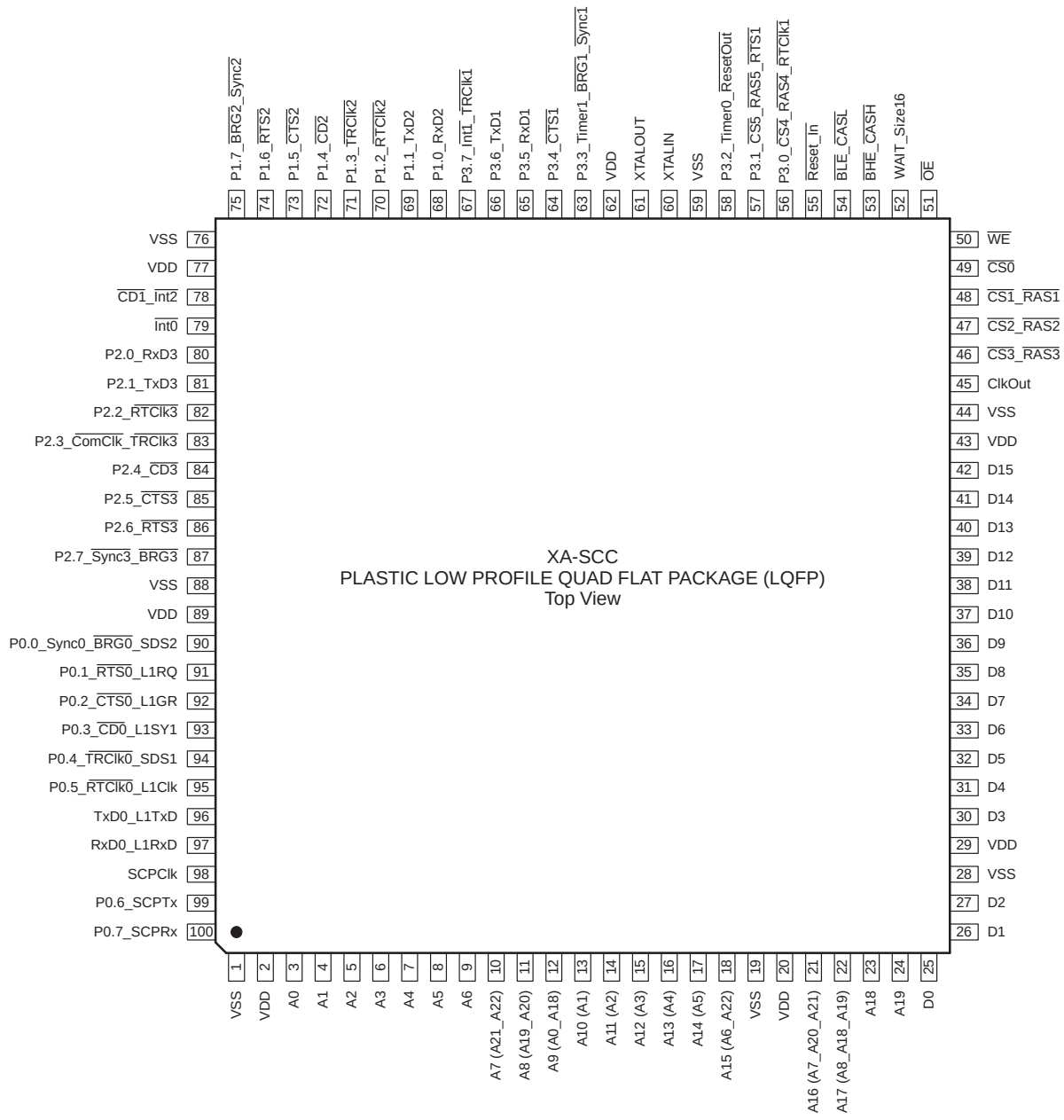
- 3.3V to 5.5V operation to 30MHz over the industrial temperature range, available in 100 pin LQFP package.
- 4 onboard SCC's for 2B+D plus Asynch port, or any combination of 4 sync/async ports. Industry standard IDL and SCP interfaces for glueless connection to U-Chip or S/T chip. Sync data rates to 4Mbps. Asynch data rates to 921.6Kbps with/without autobaud.
- Complete onboard DRAM controller supports 5 banks of up to 8MBytes each. Interfaces without glue chips to most industry standard DRAMs.
- Memory controller also generates 6 chip selects to support SRAM, ROM, Flash, EPROM, peripheral chips, etc. without external glue.
- Supports off-chip addressing up to 32 MB (2 x 2**24 address spaces) in Harvard architecture, or 16MB in unified memory configuration.
- A clock output reference "ClkOut" is added to simplify external bus interfacing.
- High performance 8-channel DMA Controller offloads the CPU for moving data to/from SCC's and memory.
- Two standard counter/timers with enhanced features (same as XA-G3 T0, T1). Both timers have a toggle output capability.
- Watchdog timer.
- Seven standard software interrupts, plus four High Priority Software Interrupts, plus 7 levels of Hardware Event Interrupts.
- Active low reset output pin indicates all internal reset occurrences (watchdog reset and the RESET instruction). A reset source register allows program determination of the cause of the most recent reset.
- 32 General Purpose I/O pins, each with 4 programmable output configurations.
- Power saving operating modes: Idle and Power-Down. Wake-Up from power-down via an external interrupt is supported.

ORDERING INFORMATION

ROMless Only	TEMPERATURE RANGE °C AND PACKAGE	FREQ (MHz)	PACKAGE DRAWING NUMBER
PXASCCKFBE	–40 to +85, 100-pin Low Profile Quad Flat Pkg. (LQFP)	30	SOT407-1

NOTE:
1. K=30MHz, F = (–40 to +85 °C), BE = LQFP

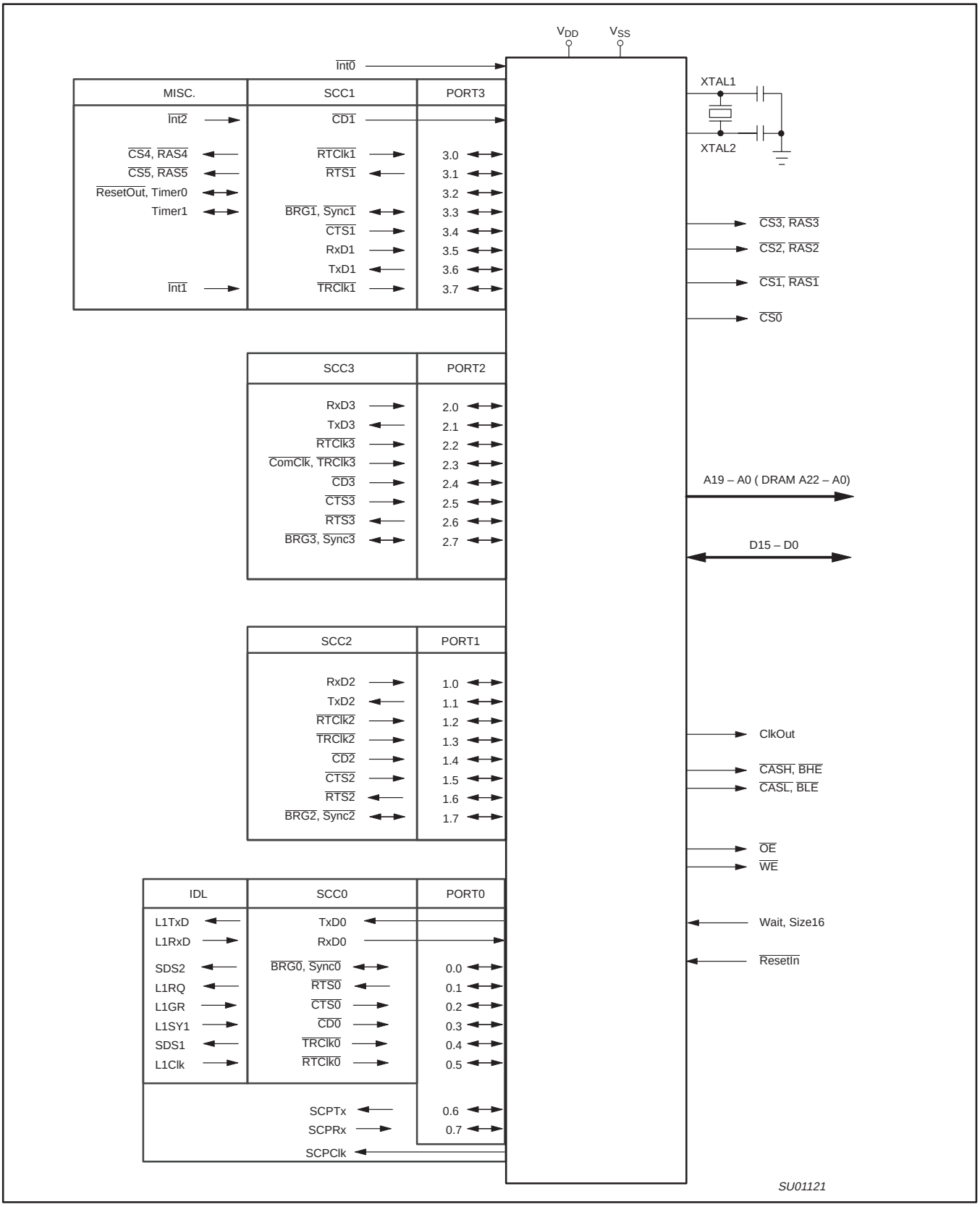
PIN CONFIGURATION



NOTE:
Address lines output during various DRAM CAS cycles are shown in parentheses.
See DRAM controller for details.

SU01120

LOGIC SYMBOL



BLOCK DIAGRAM

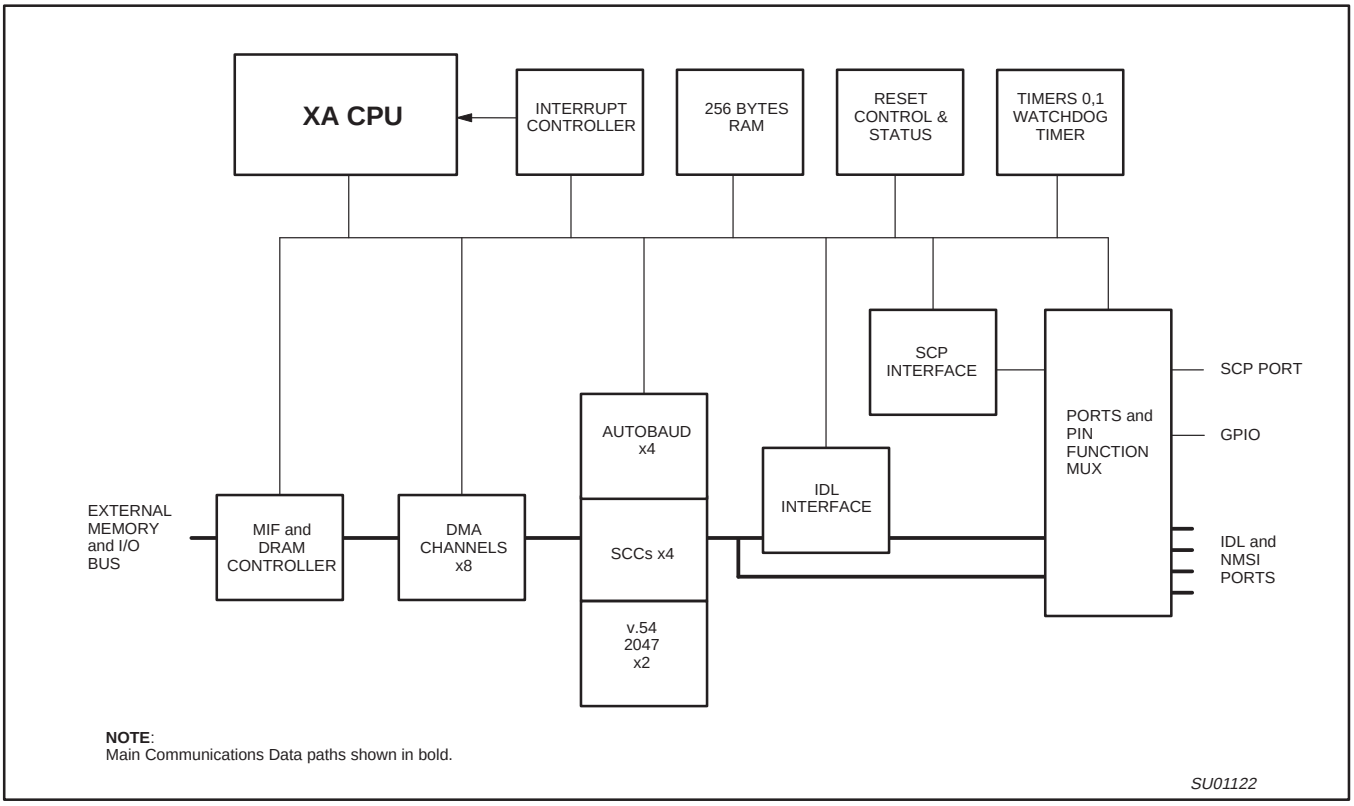


Figure 1. XA-SCC Block Diagram

PIN DESCRIPTIONS

MNEMONIC	LQFP PIN NO.	TYPE	NAME AND FUNCTION
V_{SS}	1, 19, 28, 44, 59, 76, 88	I	**Ground**: 0V reference.
V_{DD}	2, 20, 29, 43, 62, 77, 89	I	**Power Supply**: This is the power supply voltage for normal, idle, and power down operation.
$\overline{\text{ResetIn}}$	55	I	**Reset**: A low on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor to begin execution at the address contained in the reset vector.
WAIT/Size16	52	I	**Wait/Size16**: During Reset, this input determines bus size for boot device (1 = 16 bit boot device, 0 = 8 bit.) During normal operation this is the Wait input (1 = Wait, 0 = Proceed.)
XTALIn	60	I	**Crystal 1**: Input to the inverting amplifier used in the oscillator circuit and input to the internal clock generator circuits.
XTALOut	61	I	**Crystal 2**: Output from the oscillator amplifier.
$\overline{\text{CS0}}$	49	O	**Chip Select 0**: This output provides the active low chip select to the boot device (usually ROM or Flash.) It cannot be connected to DRAM. From reset, it is enabled and mapped to an address range based at 000000h. It can be remapped to a higher base in the address map (see the Memory Interface chapter in the XA-SCC User Manual.)
$\overline{\text{CS1}}$_$\overline{\text{RAS1}}$	48	O	**Chip Select 1 , RAS 1**: Chip selects 1 through 5 come out of reset disabled. They can be programmed to function as normal chip selects, or as RAS strobes to DRAM. CS1 can be “swapped” with CS0 (see the SWAP operation and control bit in the Memory Controller chapter of the XA-SCC User Manual.) CS1 is usually mapped to be based at 000000h eventually, but is capable of being based anywhere in the 16MB space.
$\overline{\text{CS2}}$_$\overline{\text{RAS2}}$	47	O	**CS2 , RAS 2**: Active low chip selects CS1 through CS5 come out of reset disabled. They can be programmed to function as normal chip selects, or as RAS strobes to DRAM. CS2 through CS5 are not used with the “SWAP” operation (see Memory Controller chapter in the XA-SCC User Manual.) They are mappable to any region of the 16MB address space.
$\overline{\text{CS3}}$_$\overline{\text{RAS3}}$	46	O	**CS3, RAS 3**: See chip select 2 for description.
see pins 56,57 for 2 more chip selects			
$\overline{\text{WE}}$	50	O	**Write Enable**: Goes active low during all bus write cycles only.
$\overline{\text{OE}}$	51	O	**Output Enable**: Goes active low during all bus read cycles only.
$\overline{\text{BLE}}$_$\overline{\text{CASL}}$	54	O	**Byte Low Enable** or **CAS_Low_Byte**: Goes active low during all bus cycles that access D7–D0, read or write, Generic or DRAM. Functions as CAS during DRAM cycles.
$\overline{\text{BHE}}$_$\overline{\text{CASH}}$	53	O	**Byte High Enable** or **CAS_High_Byte**: Goes active low during all bus cycles that access D15–D8, read or write, Generic or DRAM. Functions as CAS during DRAM cycles.
ClkOut	45	O	**Clock Output**: This pin outputs a buffered version of the internal CPU clock. The clock output may be used in conjunction with the external bus to synchronize WAIT state generators, etc. The clock output may be disabled by software. **WARNING**: The capacitive loading on this output must not exceed 40pF.
A19–A0	24–21, 18–3	O	**Address[19:0]**: These address lines output a19–a0 during generic (SRAM etc) bus cycles. DRAMs are connected only to pins 22,21, 18–10 (pins A17 to A7; see User Manual MIF Chapter for connecting various DRAM sizes); the appropriate address values are multiplexed onto these 11 pins for RAS and CAS during DRAM bus cycles.
D15–D0	42–30, 27–25	I/O	**Data[15:0]**: Bi-directional data bus, D15–D0.
P0.0[1]	90	I/O	**P0.0**_**$\overline{\text{Sync0}}$**_**$\overline{\text{BRG0}}$**_**SDS2**: Port 0 Bit 0, or SCC0 $\overline{\text{Sync}}$ input or output, or SCC0 $\overline{\text{BRG}}$ output, or $\overline{\text{SCC0}}$ $\overline{\text{TxClk}}$ output, or IDL SDS2 output.
P0.1[1]	91	I/O	**P0.1**_**$\overline{\text{RTS0}}$**_**L1RQ**: Port0 Bit1 , or SCC0 $\overline{\text{RTS}}$ (Request to send) output, or IDL L1RQ (D Channel Request) output.
P0.2[1]	92	I/O	**P0.2**_**$\overline{\text{CTS0}}$**_**L1GR**: Port 0 Bit2, or SCC0 $\overline{\text{CTS}}$ (Clear to Send) input or IDL L1GR (D Channel Grant) input
P0.3[1]	93	I/O	**P0.3**_**$\overline{\text{CD0}}$**_**L1SY1**: Port 0 Bit 3, or SCC0 Carrier Detect input, or IDL Sync input.
P0.4[1, 2]	94	I/O	**P0.4**_**$\overline{\text{TRClk0}}$**_**SDS1**: Port 0 Bit 4, or SCC0 TR clock input, or IDL SDS1 output.

MNEMONIC	LQFP PIN NO.	TYPE	NAME AND FUNCTION
P0.5[1, 2]	95	I/O	**P0.5_RTClk0_L1Clk**: Port 0 Bit 5, or SCC0 RT clock input, or IDL Clock input.
P0.6[1]	99	I/O	**P0.6_SCPTx**: Port 0 Bit 6, or SCP interface Transmit data output.
P0.7[1]	100	I/O	**P0.7_SCPRx**: Port 0 Bit 7, or SCP interface Receive data input.
TxD0_L1TxD	96	O	**TxD0_L1Txd**: Transmit data for SCC0 in NMSI mode, or for IDL bus
RxD0_L1RxD	97	I	**RxD0_L1Rxd**: Receive data for SCC0 in NMSI mode, or for IDL bus
SCPClk	98	O	**SCPClk**: This output provides the gated clock for the SCP bus.
P1.0	68	I/O	**P1.0_RxD2**: Port 1 Bit 0, or SCC2 RxD input
P1.1	69	I/O	**P1.1_TxD2**: Port 1 Bit 1, or SCC2 TxD output
P1.2[2]	70	I/O	**P1.2_$\overline{\text{RTClk2}}$**: Port 1 Bit 2, or SCC2 RT Clock input
P1.3[2]	71	I/O	**P1.3_$\overline{\text{TRClk2}}$**: Port 1 Bit 3, or SCC2 TR Clock input
P1.4	72	I/O	**P1.4_$\overline{\text{CD2}}$**: Port 1 Bit 4, or SCC2 Carrier Detect input
P1.5	73	I/O	**P1.5_$\overline{\text{CTS2}}$**: Port 1 Bit 5, or SCC2 Clear To Send input
P1.6	74	I/O	**P1.6_$\overline{\text{RTS2}}$**: Port 1 Bit 6, or SCC2 Request To Send output
P1.7	75	I/O	**P1.7_$\overline{\text{BRG2}}$_$\overline{\text{Sync2}}$**: Port 1 Bit 7, or SCC2 $\overline{\text{Sync}}$ input or output, or BRG output, or TxClk output (see SCC clocks diagrams in User Manual Chp 5)
P2.0	80	I/O	**P2.0_RxD3**: Port 2 Bit 0, or SCC3 Rx Data input
P2.1	81	I/O	**P2.1_TxD3**: Port 2 Bit 1, or SCC3 Tx Data output
P2.2[2]	82	I/O	**P2.2_$\overline{\text{RTClk3}}$**: Port 2 Bit 2, or SCC3 RT Clock input
P2.3[2]	83	I/O	**P2.3_ComClk_$\overline{\text{TRClk3}}$**: Port 2 Bit 3, or SCC3 TR Clock input
P2.4	84	I/O	**P2.4_$\overline{\text{CD3}}$**: Port 2 Bit 4, or SCC3 Carrier Detect input
P2.5	85	I/O	**P2.5_$\overline{\text{CTS3}}$**: Port 2 Bit 5, or SCC3 Clear To Send input
P2.6	86	I/O	**P2.6_$\overline{\text{RTS3}}$**: Port 2 Bit 6, or SCC3 Request To Send output
P2.7	87	I/O	**P2.7_Sync3_BRG3**: Port 2 Bit 7, or SCC3 $\overline{\text{Sync}}$ input or output, or $\overline{\text{BRG}}$ output, or $\overline{\text{TxClk}}$ output (see SCC clocks diagrams in User Manual Chp 5)
P3.0[2]	56	I/O	**P3.0_$\overline{\text{CS4}}$_$\overline{\text{RAS4}}$_$\overline{\text{RTClk1}}$**: Port 3 Bit 0, or $\overline{\text{CS4}}$ or $\overline{\text{RAS4}}$ output, or SCC1 $\overline{\text{RT Clock}}$ input
P3.1	57	I/O	**P3.1_$\overline{\text{CS5}}$_$\overline{\text{RAS5}}$_$\overline{\text{RTS1}}$**: Port 3 Bit 1, or $\overline{\text{CS5}}$ or $\overline{\text{RAS5}}$ output, or SCC1 $\overline{\text{Request To Send}}$ output
P3.2	58	I/O	**P3.2_Timer0_$\overline{\text{ResetOut}}$**: Port 3 Bit 2, or Timer0 input or output, or $\overline{\text{ResetOut}}$ output. **$\overline{\text{ResetOut}}$**: If the $\overline{\text{ResetOut}}$ function is selected, this pin outputs a low whenever the XA-SCC processor is reset by an **internal** source (watchdog reset or the RESET instruction.) **WARNING**: Unlike the other 31 GPIO pins, during power up reset, this pin can output a strongly driven low pulse. The duration of this low pulse ranges from 0ns to 258 system clocks, starting at the time that V_{CC} is valid. The state of the $\overline{\text{ResetIn}}$ pin does not affect this pulse. When used as GPIO, this pin can also be driven low by software without resetting the XA-SCC.
P3.3	63	I/O	**P3.3_Timer1_$\overline{\text{BRG1}}$_$\overline{\text{Sync1}}$**: Port 3 Bit 3, or Timer1 input or output, or SCC1 $\overline{\text{BRG}}$ output, or SCC1 $\overline{\text{Sync}}$ input or output
P3.4	64	I/O	**P3.4_$\overline{\text{CTS1}}$**: Port 3 Bit 4, or SCC1 $\overline{\text{Clear To Send}}$ input
P3.5	65	I/O	**P3.5_RxD1**: Port 3 Bit 5, or SCC1 Receive Data input
P3.6	66	I/O	**P3.6_TxD1**: Port 3 Bit 6, or SCC1 Transmit Data output
P3.7[2]	67	I/O	**P3.7_$\overline{\text{Int1}}$_$\overline{\text{TRClk1}}$**: Port 3 Bit 7, or $\overline{\text{External Interrupt1}}$ input, or SCC1 $\overline{\text{TR Clock}}$ input
$\overline{\text{CD1}}$_$\overline{\text{Int2}}$	78	I	**$\overline{\text{CD1}}$_$\overline{\text{Int2}}$**: SCC1 $\overline{\text{Carrier Detect}}$, or $\overline{\text{External Interrupt 2}}$
$\overline{\text{Int0}}$	79	I	**$\overline{\text{External Interrupt 0}}$**

NOTES:
1. See XA-SCC User Guide “Pins Chapter” for how to program selection of pin functions.
2. RTClk input is usually used for Rx Clock if an external clock is needed, but can be used for either Rx or Tx or both. TRClk is usually used for Tx Clock, but can be used for Rx or Tx or both.

CONTROL REGISTER OVERVIEW

There are two types of control registers in the XA-SCC, these are SFRs (Special Function Registers), and MMRs (Memory Mapped Registers.) The SFR registers, with the exception of MRBL, MRBH, MICFG, BCR, BRTH, BRTL, and RSTSRC are the standard XA core registers. See **WARNINGs about BCR, BRTH, and BRTL in the Table below.**

SFRs are accessed by “direct addressing” only (see IC25 XA User Manual for direct addressing.) The MMRs are specific to the XA-SCC on board peripherals, and can be accessed by any addressing mode that can be used for off chip data accesses. The MMRs are implemented in a relocatable block. See the MIF chapter in the XA-SCC User Manual for details on how to relocate the MMRs by writing a new base address into the MRBL and MRBH (MMR Base Low and High) registers.

Table 1. Special Function Registers (SFR)[1, 2, 3]

NAME	DESCRIPTION	SFR Address	BIT FUNCTIONS AND ADDRESSES MSB							LSB	RESET VALUE
BCR	Bus Configuration Reg RESERVED—see warning	46Ah	**WARNING—Never write to the BCR register in the XA-SCC part—it is initialized to 07h, the only legal value. This is not the same as for other XA derivatives.**								07h
BTRH	Bus Timing Reg High	469h	**WARNING—Immediately after reset, always write BTRH = 51h, followed by writing BTRL = 40h in that order. Follow these two writes with five NOPS. This is not the same as for other XA derivatives.**								FFh
BTRL	Bus Timing Reg Low	468h									EFh
MRBL#	MMR Base Address Low	496h	MA15	MA14	MA13	MA12	–	–	–	MRBE	x0h
MRBH#	MMR Base Address High	497h	MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16	xx
MICFG#	ClkOut Tri-St Enable 1 = Enabled	499h	–	–	–	–	–	–	–	CLKOE	01h
CS	Code Segment	443h									00h
DS	Data Segment	441h									00h
ES	Extra Segment	442h									00h
			33F	33E	33D	33C	33B	33A	339	338	
IEH*	Interrupt Enable High	427h	EHSWR3	EHSWR2	EHSWR1	EHSWR0	ESCP	EAuto	ESC23	ESC01	00h
			337	336	335	334	333	332	331	330	
IEL*	Interrupt Enable Low	426h	EA	EDMAH	EDMAL	EX2	ET1	EX1	ET0	EX0	00h
IPA0	Interrupt Priority A0	4A0h	–	PT0			–	PX0			00h
IPA1	Interrupt Priority A1	4A1h	–		PT1		–	PX1			00h
IPA2	Interrupt Priority A2	4A2h	–	PDMAL			–	PX2			00h
IPA3	Interrupt Priority A3	4A3h	Reserved				–	PDMAH			00h
IPA4	Interrupt Priority A4	4A4h	–	PSC23			–	PSC01			00h
IPA5	Interrupt Priority A5	4A5h	–	PSCP			–	PAutoB			00h
IPA6	Interrupt Priority A6	4A6h	–	PHSWR1			–	PHSWR0			00h
IPA7	Interrupt Priority A7	4A7h	–	PHSWR3			–	PHSWR2			00h
			387	386	385	384	383	382	381	380	
P0*	Port 0	430h									FFh
			38F	38E	38D	38C	38B	38A	389	388	
P1*	Port 1	431h									FFh
			397	396	395	394	393	392	391	390	
P2*	Port 2	432h									FFh

NAME	DESCRIPTION	SFR Address	BIT FUNCTIONS AND ADDRESSES MSB							LSB	RESET VALUE
			39F	39E	39D	39C	39B	39A	399	398	
P3*	Port 3	433h									FFh
P0CFGA	Port 0 Configuration A	470h									Note 4
P1CFGA	Port 1 Configuration A	471h									Note 4
P2CFGA	Port 2 Configuration A	472h									Note 4
P3CFGA	Port 3 Configuration A	473h									Note 4
P0CFGB	Port 0 Configuration B	4F0h									Note 4
P1CFGB	Port 1 Configuration B	4F1h									Note 4
P2CFGB	Port 2 Configuration B	4F2h									Note 4
P3CFGB	Port 3 Configuration B	4F3h									Note 4
			227	226	225	224	223	222	221	220	
PCON*	Power Control Reg	404h	–	–	–	–	–	–	PD	IDL	00h
			20F	20E	20D	20C	20B	20A	209	208	
PSWH*	Program Status Word High	401h	SM	TM	RS1	RS0	IM3	IM2	IM1	IM0	Note 5
			207	206	205	204	203	202	201	200	
PSWL*	Program Status Word Low	400h	C	AC	–	–	–	V	N	Z	Note 5
			217	216	215	214	213	212	211	210	
PSW51*	80C51 compatible PSW	402h	C	AC	F0	RS1	RS0	V	F1	P	Note 6
RSTSRC	Reset Source Reg	463h	ROEN	–	–	–	–	R_WD	R_CMD	R_EXT	Note 7
RTH0	Timer 0 Reload High	455h									00h
RTH1	Timer 1 Reload High	457h									00h
RTL0	Timer 0 Reload Low	454h									00h
RTL1	Timer 1 Reload Low	456h									00h
SCR	System Configuration Reg	440h	–	–	–	–	PT1	PT0	CM	PZ	00h
			21F	21E	21D	21C	21B	21A	219	218	
SSEL*	Segment Selection Reg	403h	ESWEN	R6SEG	R5SEG	R4SEG	R3SEG	R2SEG	R1SEG	R0SEG	00h

NAME	DESCRIPTION	SFR Address	BIT FUNCTIONS AND ADDRESSES MSB							LSB	RESET VALUE
SWE	Software Interrupt Enable	47Ah	–	SWE7	SWE6	SWE5	SWE4	SWE3	SWE2	SWE1	00h
			357	356	355	354	353	352	351	350	
SWR*	Software Interrupt Request	42Ah	–	SWR7	SWR6	SWR5	SWR4	SWR3	SWR2	SWR1	00h
			287	286	285	284	283	282	281	280	
TCON*	Timer 0/1 Control	410h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
TH0	Timer 0 High	451h									00h
TH1	Timer 1 High	453h									00h
TL0	Timer 0 Low	450h									00h
TL1	Timer 1 Low	452h									00h
TMOD	Timer 0/1 Mode	45Ch	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
			28F	28E	28D	28C	28B	28A	289	288	
TSTAT*	Timer 0/1 Extended Status	411h	–	–	–	–	–	T1OE	–	T0OE	00h
			2FF	2FE	2FD	2FC	2FB	2FA	2F9	2F8	
WDCON*	Watchdog Control	41Fh	PRE2	PRE1	PRE0	–	–	WDRUN	WDTOF	–	Note 8
WDL	Watchdog Timer Reload	45Fh									00h
WFEED1	Watchdog Feed 1	45Dh									xx
WFEED2	Watchdog Feed 2	45Eh									xx

NOTES:

* SFRs marked with an asterisk (*) are bit addressable.

\# SFRs marked with a pound sign (#) are additional SFR registers specific to the XA-SCC.

1. The XA-SCC implements an 8-bit SFR bus, as stated in Chapter 8 of the IC25 Data Handbook XA User Guide. All SFR accesses must be 8-bit operations. Attempts to write 16 bits to an SFR will actually write only the lower 8 bits. Sixteen bit SFR reads will return undefined data in the upper byte.
2. Unimplemented bits in SFRs are X (unknown) at all times. Ones should not be written to these bits since they may be used for other purposes in future XA derivatives. The reset value shown for these bits is 0.
3. The XA guards writes to certain bits (typically interrupt flags) that may be written by a peripheral function. This prevents loss of an interrupt or other status if a bit was written directly by a peripheral action between the read and write of an instruction that performs a read-modify-write operation. XA-SCC SFR bits that are guarded in this manner are: TF1, TF0, IE1, and IE0 (in TCON), and WDTOF (in WDCON).
4. Port configurations default to quasi-bidirectional when the XA begins execution after reset. Thus all PnCFGA registers will contain FFh and PnCFGB register will contain 00h. See warning in XA-SCC User Manual about P3.2_Timer0_$\overline{\text{ResetOut}}$ pin during first 258 clocks after power up. Basically, during this period, this pin may output a strongly driven low pulse. If the pulse does occur, it will terminate in a transition to high at a time no later than the 259th system clock after valid VCC power up.
5. SFR is loaded from the reset vector.
6. F1, F0, and P reset to 0. All other bits are loaded from the reset vector.
7. The RSTSRC register reflects the cause of the last XA reset. One bit will be set to 1, the others will be 0. RSTSRC[7] enables the $\overline{\text{ResetOut}}$ function; 1 = Enabled, 0 = Disabled. See XA-SCC User Manual for details; RSTSRC[7] differs in function from most other XA derivatives.
8. The WDCON reset value is E6 for a Watchdog reset, E4 for all other reset causes.

Table 2. Memory Mapped Registers

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
SCCO Registers					
SCC0 Write Register 0	R/W	8	800h	Command register	00h
SCC0 Write Register 1	R/W	8	802h	Tx/Rx Interrupt & data transfer mode	xx
SCC0 Write Register 2	R/W	8	804h	Extended Features Control	xx
SCC0 Write Register 3	R/W	8	806h	Receive Parameter and Control	00h
SCC0 Write Register 4	R/W	8	808h	Tx/Rx misc. parameters & mode	00h
SCC0 Write Register 5	R/W	8	80Ah	Tx. parameter and control	00h
SCC0 Write Register 6	R/W	8	80Ch	Sync character or SDLC address field or Match Character 0	00h
SCC0 Write Register 7	R/W	8	80Eh	Sync character or SDLC flag or Match Character 1	xx
SCC0 Write Register 8	R/W	8	810h	Transmit Data Buffer	xx
SCC0 Write Register 9	R/W	8	812h	Master Interrupt control	xx
SCC0 Write Register 10	R/W	8	814h	Misc. Tx/Rx control register	00h
SCC0 Write Register 11	R/W	8	816h	Clock Mode Control	xx
SCC0 Write Register 12	R/W	8	818h	Lower Byte of Baud rate time constant	00h
SCC0 Write Register 13	R/W	8	81Ah	Upper Byte of Baud rate time constant	00h
SCC0 Write Register 14	R/W	8	81Ch	Misc. Control bits	xx
SCC0 Write Register 15	R/W	8	81Eh	External/Status interrupt control	f8h
SCC0 Write Register 16	R/W	8	828h	Match Character 2 (WR16)	00h
SCC0 Write Register 17	R/W	8	82Ah	Match Character 3 (WR17)	00h
SCC0 Read Register 0	RO	8	820h	Tx/Rx buffer and external status	—
SCC0 Read Register 1	RO	8	822h	Receive condition status/residue code	—
Reserved—do not write			824h		—
SCC0 Read Register 3	RO	8	826h	Interrupt Pending Bits	—
see WR16 and 17			828–82Ah	see WR16 and WR17 above	—
SCC0 Read Register 6	RO	8	82Ch	SDLC byte count low register	—
SCC0 Read Register 7	RO	8	82Eh	SDLC byte count high & FIFO status	—
SCC0 Read Register 8	RO	8	830h	Receive Buffer	—
Reserved			832h		—
SCC0 Read Register 10	RO	8	834h	Loop/clock status	—
Reserved			836–83Eh		—
SCC1 Registers					
SCC1 Write Register 0	R/W	8	840h	Command register	00h
SCC1 Write Register 1	R/W	8	842h	Tx/Rx Interrupt & data transfer mode	xx
SCC1 Write Register 2	R/W	8	844h	Extended Features Control	xx
SCC1 Write Register 3	R/W	8	846h	Receive Parameter and Control	00h
SCC1 Write Register 4	R/W	8	848h	Tx/Rx misc. parameters & mode	00h
SCC1 Write Register 5	R/W	8	84Ah	Tx. parameter and control	00h
SCC1 Write Register 6	R/W	8	84Ch	Sync character or SDLC address field or Match Character 0	00h
SCC1 Write Register 7	R/W	8	84Eh	Sync character or SDLC flag or Match Character 1	xx
SCC1 Write Register 8	R/W	8	850h	Transmit Data Buffer	xx
SCC1 Write Register 9	R/W	8	852h	Master Interrupt control	xx
SCC1 Write Register 10	R/W	8	854h	Misc. Tx/Rx control register	00h
SCC1 Write Register 11	R/W	8	856h	Clock Mode Control	xx
SCC1 Write Register 12	R/W	8	858h	Lower Byte of Baud rate time constant	00h

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
SCC1 Write Register 13	R/W	8	85Ah	Upper Byte of Baud rate time constant	00h
SCC1 Write Register 14	R/W	8	85Ch	Misc. Control bits	xx
SCC1 Write Register 15	R/W	8	85Eh	External/Status interrupt control	f8h
SCC1 Write Register 16	R/W	8	868h	Match Character 2 (WR16)	00h
SCC1 Write Register 17	R/W	8	86Ah	Match Character 3 (WR17)	00h
SCC1 Read Register 0	RO	8	860h	Tx/Rx buffer and external status	—
SCC1 Read Register 1	RO	8	862h	Receive condition status/residue code	—
Reserved			864h		—
SCC1 Read Register 3	RO	8	866h	Interrupt Pending Bits	—
see WR16 and 17			868–86Ah	see WR16 and WR17 above	—
SCC1 Read Register 6	RO	8	86Ch	SDLC byte count low register	—
SCC1 Read Register 7	RO	8	86Eh	SDLC byte count high & FIFO status	—
SCC1 Read Register 8	RO	8	870h	Receive Buffer	—
Reserved			872h		—
SCC1 Read Register 10	RO	8	874h	Loop/clock status	—
Reserved			876–87Eh		—
SCC2 Registers					
SCC2 Write Register 0	R/W	8	880h	Command register	00h
SCC2 Write Register 1	R/W	8	882h	Tx/Rx Interrupt & data transfer mode	xx
SCC2 Write Register 2	R/W	8	884h	Extended Features Control	xx
SCC2 Write Register 3	R/W	8	886h	Receive Parameter and Control	00h
SCC2 Write Register 4	R/W	8	888h	Tx/Rx misc. parameters & mode	00h
SCC2 Write Register 5	R/W	8	88Ah	Tx. parameter and control	00h
SCC2 Write Register 6	R/W	8	88Ch	Sync character or SDLC address field or Match Character 0	00h
SCC2 Write Register 7	R/W	8	88Eh	Sync character or SDLC flag or Match Character 1	xx
SCC2 Write Register 8	R/W	8	890h	Transmit Data Buffer	xx
SCC2 Write Register 9	R/W	8	892h	Master Interrupt control	xx
SCC2 Write Register 10	R/W	8	894h	Misc. Tx/Rx control register	00h
SCC2 Write Register 11	R/W	8	896h	Clock Mode Control	xx
SCC2 Write Register 12	R/W	8	898h	Lower Byte of Baud rate time constant	00h
SCC2 Write Register 13	R/W	8	89Ah	Upper Byte of Baud rate time constant	00h
SCC2 Write Register 14	R/W	8	89Ch	Misc. Control bits	xx
SCC2 Write Register 15	R/W	8	89Eh	External/Status interrupt control	f8h
SCC2 Write Register 16	R/W	8	8A8h	Match Character 2 (wr16)	00h
SCC2 Write Register 17	R/W	8	8AAh	Match Character 3 (wr17)	00h
SCC2 Read Register 0	RO	8	8A0h	Tx/Rx buffer and external status	—
SCC2 Read Register 1	RO	8	8A2h	Receive condition status/residue code	—
Reserved			8A4h		—
SCC2 Read Register 3	RO	8	8A6h	Interrupt Pending Bits	—
see WR16 and 17			8A8–8AAh	see WR16 and WR17 above	—
SCC2 Read Register 6	RO	8	8ACh	SDLC byte count low register	—
SCC2 Read Register 7	RO	8	8AEh	SDLC byte count high & FIFO status	—
SCC2 Read Register 8	RO	8	8B0h	Receive Buffer	—
Reserved			8B2h		—
SCC2 Read Register 10	RO	8	8B4h	Loop/clock status	—
Reserved			8B6–8BEh		—

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
SCC3 Registers					
SCC3 Write Register 0	R/W	8	8C0h	Command register	00h
SCC3 Write Register 1	R/W	8	8C2h	Tx/Rx Interrupt & data transfer mode	xx
SCC3 Write Register 2	R/W	8	8C4h	Extended Features Control	xx
SCC3 Write Register 3	R/W	8	8C6h	Receive Parameter and Control	00h
SCC3 Write Register 4	R/W	8	8C8h	Tx/Rx misc. parameters & mode	00h
SCC3 Write Register 5	R/W	8	8CAh	Tx. parameter and control	00h
SCC3 Write Register 6	R/W	8	8CCh	Sync character or SDLC address field or Match Character 0	00h
SCC3 Write Register 7	R/W	8	8CEh	Sync character or SDLC flag or Match Character 1	xx
SCC3 Write Register 8	R/W	8	8D0h	Transmit Data Buffer	xx
SCC3 Write Register 9	R/W	8	8D2h	Master Interrupt control	xx
SCC3 Write Register 10	R/W	8	8D4h	Misc. Tx/Rx control register	00h
SCC3 Write Register 11	R/W	8	8D6h	Clock Mode Control	xx
SCC3 Write Register 12	R/W	8	8D8h	Lower Byte of Baud rate time constant	00h
SCC3 Write Register 13	R/W	8	8DAh	Upper Byte of Baud rate time constant	00h
SCC3 Write Register 14	R/W	8	8DCh	Misc. Control bits	xx
SCC3 Write Register 15	R/W	8	8DEh	External/Status interrupt control	f8h
SCC3 Write Register 16	R/W	8	8E8h	Match Character 2 (wr16)	00h
SCC3 Write Register 17	R/W	8	8EAh	Match Character 3 (wr17)	00h
SCC3 Read Register 0	RO	8	8E0h	Tx/Rx buffer and external status	—
SCC3 Read Register 1	RO	8	8E2h	Receive condition status/residue code	—
Reserved			8E4h		—
SCC3 Read Register 3	RO	8	8E6h	Interrupt Pending Register	—
SCC3 Read Register 6	RO	8	8ECh	SDLC byte count low register	—
SCC3 Read Register 7	RO	8	8EEh	SDLC byte count high & FIFO status	—
SCC3 Read Register 8	RO	8	8F0h	Receive Buffer	—
Reserved			8F2h		—
SCC3 Read Register 10	RO	8	8F4h	Loop/clock status	—
Reserved			8F6–8FEh		—
Rx DMA Registers					
DMA Control Register Ch.0 Rx	R/W	8	100h	Control Register	00h
FIFO Control & Status Reg Ch.0 Rx	R/W	8	101h	Control & Status Register	00h
Segment Register Ch.0 Rx	R/W	8	102h	Points to 64K data segment	00h
Buffer Base Register Ch.0 Rx	R/W	8	104h	Wrap Reload Value for A15 –A8, A7–A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.0 Rx	R/W	16	106h	Upper Bound (plus 1) on A15–A0	0000h
Address Pointer Reg Ch.0 Rx	R/W	16	108h	Current Address pointer A15–A0	0000h
Byte Count Register Ch.0 Rx	R/W	16	10Ah	Corresponds to A15–A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.0 Lo Rx	R/W	16	10Ch	10Ch = Byte 0 = older, 10Dh = Byte 1 = younger	00h 00h
Data FIFO Register Ch.0 Hi Rx	R/W	16	10Eh	10Eh = Byte 2 = older, 10Fh = Byte 3 = younger	00h 00h
DMA Control Register Ch.1 Rx	R/W	8	110h	Control Register	00h
FIFO Control & Status Register Ch.1 Rx	R/W	8	111h	Control & Status Register	00h
Segment Register Ch. 1 Rx	R/W	8	112h	Points to 64K data segment	00h
Buffer Base Register Ch. 1 Rx	R/W	8	114h	Wrap Reload Value for A15 –A8, A7–A0 reloaded to zero by hardware	00h

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
Buffer Bound Register Ch.1 Rx	R/W	16	116h	Upper Bound (plus 1) on A15–A0	0000h
Address Pointer Reg Ch.1 Rx	R/W	16	118h	Current Address pointer A15–A0	0000h
Byte Count Register Ch.1 Rx	R/W	16	11Ah	Corresponds to A15–A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.1 Lo Rx	R/W	16	11Ch	11Ch = Byte 0 = older, 11Dh = Byte 1 = younger	00h 00h
Data FIFO Register Ch.1 Hi Rx	R/W	16	11Eh	11Eh = Byte 2 = older, 11Fh = Byte 3 = younger	00h 00h
DMA Control Register Ch.2 Rx	R/W	8	120h	Control Register	00h
FIFO Control & Status Register Ch.2 Rx	R/W	8	121h	Control & Status Register	00h
Segment Register Ch. 2 Rx	R/W	8	122h	Points to 64K data segment	00h
Buffer Base Register Ch. 2 Rx	R/W	8	124h	Wrap Reload Value for A15 –A8, A7–A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.2 Rx	R/W	16	126h	Upper Bound (plus 1) on A15–A0	0000h
Address Pointer Reg Ch.2 Rx	R/W	16	128h	Current Address pointer A15–A0	0000h
Byte Count Register Ch.2 Rx	R/W	16	12Ah	Corresponds to A15–A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.2 Lo Rx	R/W	16	12Ch	12Ch = Byte 0 = older, 12Dh = Byte 1 = younger	00h 00h
Data FIFO Register Ch.2 Hi Rx	R/W	16	12Eh	12Eh = Byte 2 = older, 12Fh = Byte 3 = younger	00h 00h
DMA Control Register Ch.3 Rx	R/W	8	130h	Control Register	00h
FIFO Control & Status Register Ch.3 Rx	R/W	8	131h	Control & Status Register	00h
Segment Register Ch. 3 Rx	R/W	8	132h	Points to 64K data segment	00h
Buffer Base Register Ch. 3 Rx	R/W	8	134h	Wrap Reload Value for A15 –A8, A7–A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.3 Rx	R/W	16	136h	Upper Bound (plus 1) on A15–A0	0000h
Address Pointer Reg Ch.3 Rx	R/W	16	138h	Current Address pointer A15–A0	0000h
Byte Count Register Ch.3 Rx	R/W	16	13Ah	Corresponds to A15–A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.3 Lo Rx	R/W	16	13Ch	13Ch = Byte 0 = older, 13Dh = Byte 1 = younger	00h 00h
Data FIFO Register Ch.3 Hi Rx	R/W	16	13Eh	13Eh = Byte 2 = older, 13Fh = Byte 3 = younger	00h 00h
Tx DMA Registers					
DMA Control Register Ch.0 Tx	R/W	8	140h	Control Register	00h
FIFO Control & Status Register Ch.0 Tx	R/W	8	141h	Control & Status Register	00h
Segment Register Ch. 0 Tx	R/W	8	142h	Points to 64K data segment	00h
Buffer Base Register Ch. 0 Tx	R/W	8	144h	Wrap Reload Value for A15 –A8, A7–A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.0 Tx	R/W	16	146h	Upper Bound (plus 1) on A15–A0	0000h
Address Pointer Reg Ch.0 Tx	R/W	16	148h	Current Address pointer A15–A0	0000h
Byte Count Register Ch.0 Tx	R/W	16	14Ah	Corresponds to A15–A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.0 Tx	R/W	16	14Ch	14C = Byte0 = older 14D = Byte 1 = younger	0000h
Data FIFO Register Ch.0 Tx	R/W	16	14Eh	14E = Byte2 = older 14F = Byte3 = younger	0000h
DMA Control Register Ch.1 Tx	R/W	8	150h	Control Register	00h
FIFO Control & Status Register Ch.1 Tx	R/W	8	151h	Control & Status Register	00h
Segment Register Ch.1 Tx	R/W	8	152h	Points to 64K data segment	00h

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
Buffer Base Register Ch.1 Tx	R/W	8	154h	Wrap Reload Value for A15–A8, A7–A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.1 Tx	R/W	16	156h	Upper Bound (plus 1) on A15–A0	0000h
Address Pointer Reg Ch.1 Tx	R/W	16	158h	Current Address pointer A15–A0	0000h
Byte Count Register Ch.1 Tx	R/W	16	15Ah	Corresponds to A15–A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.1 Lo Tx	R/W	16	15Ch	Byte0 & 1	0000h
Data FIFO Register Ch.1 Hi Tx	R/W	16	15Eh	Byte2 & 3	0000h
DMA Control Register Ch.2 Tx	R/W	8	160h	Control Register	00h
FIFO Control & Status Register Ch.2 Tx	R/W	8	161h	Control & Status Register	00h
Segment Register Ch.2 Tx	R/W	8	162h	Points to 64K data segment	00h
Buffer Base Register Ch.2 Tx	R/W	8	164h	Wrap Reload Value for A15 –A8, A7–A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.2 Tx	R/W	16	166h	Upper Bound (plus 1) on A15–A0	0000h
Address Pointer Reg Ch.2 Tx	R/W	16	168h	Current Address pointer A15–A0	0000h
Byte Count Register Ch.2 Tx	R/W	16	16Ah	Corresponds to A15–A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.2 Lo Tx	R/W	16	16Ch	Byte0 & 1	0000h
Data FIFO Register Ch.2 Hi Tx	R/W	16	16Eh	Byte2 & 3	0000h
DMA Control Register Ch.3 Tx	R/W	8	170h	Control Register	00h
FIFO Control & Status Register Ch.3 Tx	R/W	8	171h	Control & Status Register	00h
Segment Register Ch. 3 Tx	R/W	8	172h	Points to 64K data segment	00h
Buffer Base Register Ch. 3 Tx	R/W	8	174h	Wrap Reload Value for A15 –A8 A7–A0 reloaded to zero by hardware	00h
Buffer Bound Register Ch.3 Tx	R/W	16	176h	Upper Bound (plus 1) on A15–A0	0000h
Address Pointer Reg Ch.3 Tx	R/W	16	178h	Current Address pointer A15–A0	0000h
Byte Count Register Ch.3 Tx	R/W	16	17Ah	Corresponds to A15–A0 Byte Count, generates interrupt if enabled and byte count exceeded.	0000h
Data FIFO Register Ch.3Lo Tx	R/W	16	17Ch	Byte0 & 1	0000h
Data FIFO Register Ch.3 Hi Tx	R/W	16	17Eh	Byte2 & 3	0000h
	R/W		180–1FEh	RESERVED for future DMA	—
Miscellaneous DMA Registers					
Rx Character Time Out Register Ch.0	R/W	8	200h	0 value disables counter interrupt.	00h
Rx Character Time Out Register Ch.1	R/W	8	202h	Same as above, for Rx1	00h
Rx Character Time Out Register Ch.2	R/W	8	204h	Same as above, for Rx2	00h
Rx Character Time Out Register Ch.3	R/W	8	206h	Same as above, for Rx3	00h
Global DMA Interrupt Register	R/W	16	210h	DMA Interrupt Flags	0000h
V.54/2047 Registers					
VACS	R/W	8	240h	V.54 2047 Unit A Control & Status	00h
VACFG	R/W	8	241h	V.54 2047 Unit A Configuration	—
VATCL	R/W	8	242h	V.54 2047 Unit A Threshold Cntr Lo	—
VATCH	R/W	8	243h	V.54 2047 Unit A Threshold Cntr Hi	—
VAEC	R/W	8	244h	V.54 2047 Unit A Error Counter	—
VBCS	R/W	8	248h	V.54 2047 Unit B Control & Status	00h
VBCFG	R/W	8	249h	V.54 2047 Unit B Configuration	—
VBTCL	R/W	8	24Ah	V.54 2047 Unit B Threshold Cntr Lo	—
VBTCH	R/W	8	24Bh	V.54 2047 Unit B Threshold Cntr Hi	—
VBEC	R/W	8	24Ch	V.54 2047 Unit B Error Counter	—

MMR Name	Read/Write or Read Only	Size	Address Offset	Description	Reset Value
SCP Interface Registers					
SCPCFG	R/W	8	260h	SCP Configuration	8xh
SCPD	R/W	8	262h	SCP Data Byte	xx
SCPCS	R/W	8	263h	SCP Control & Status	00h
Autobaud Registers					
BDAEE	R/W	8	270h	Autobaud Echo Enable	00h ..
BDCS	R/W	8	272h	Autobaud Control & Status	00h ..
Memory Interface (MIF) Registers					
B0CFG	R/W	8	280h	MIF Bank 0 Config	—
B0AM	R/W	8	281h	MIF Bank 0 Base Address	00h..
B0TMG	R/W	8	282h	MIF Bank 0 Timing Params	—
B1CFG	R/W	8	284h	MIF Bank 1 Config	0xh
B1AM	R/W	8	285h	MIF Bank 1 Base Address	xxh
B1TMG	R/W	8	286h	MIF Bank 1 Timing Params	xxh
B2CFG	R/W	8	288h	MIF Bank 2 Config	0xh
B2AM	R/W	8	289h	MIF Bank 2 Base Address	xx
B2TMG	R/W	8	28Ah	MIF Bank 2 Timing Params	xx
B3CFG	R/W	8	28Ch	MIF Bank 3 Config	0xh
B3AM	R/W	8	28Dh	MIF Bank 3 Base Address	xx
B3TMG	R/W	8	28Eh	MIF Bank 3 Timing Params	xx
B4CFG	R/W	8	290h	MIF Bank 4 Config	0xh
B4AM	R/W	8	291h	MIF Bank 4 Base Address	xx
B4TMG	R/W	8	292h	MIF Bank 4 Timing Params	xx
B5CFG	R/W	8	294h	MIF Bank 5 Config	0xh
B5AM	R/W	8	295h	MIF Bank 5 Base Address	xx
B5TMG	R/W	8	296h	MIF Bank 5 Timing Params	xx
MBCL	R/W	8	2BEh	MIF Memory Bank Configuration Lock Register	3Fh
RFSH	R/W	8	2BFh	MIF Refresh Control	00h
IDL Interface Registers					
MSI Control Register	R/W	16	2C0h	IDL Mode Control Register	0000h
DataMask Register	R/W	16	2C2h	IDL Mask Register	0000h
Miscellaneous Registers					
Hi-Pri Soft Ints & Pin Mux Control Reg.	R/W	16	2D0h	Control bits for Hi-Priority Soft Ints, and Pin Mux	0000h
XInt2	R/W	8	2D2h	External Interrupt 2 Control	00h

FUNCTIONAL DESCRIPTION

The XA-SCC functions are described in the following sections. Because all blocks are thoroughly documented in either the IC25 XA Data Handbook, or the XA-SCC User Manual, only brief descriptions are given in this datasheet, in conjunction with references to the appropriate document.

XA CPU

The CPU is a 30MHz implementation of the standard XA CPU core. See the XA Data Handbook (IC25) for details. The CPU core is identical to the G3 core. See caveat in next paragraph about the Bus Interface Unit.

Bus Interface Unit (BIU)

This is the internal Bus, not the bus at the pins. This internal bus connects the CPU to the MIF (Memory and DRAM Controller.)

WARNING: Immediately after reset, always write BTRH = 51h, followed by BTRL = 40h, in that order. Once written, do not change the values in these registers. Follow these two writes with five NOPS. Never write to the BCR register, it comes out of reset initialized to 07h, which is the only value that will work.

Timers 0 and 1

Timers 0 and 1 are the standard XA-G3 timer 0 and 1. Each has an associated I/O pin and interrupt. See the XA-G3 data sheet in the IC25 XA Data Handbook for details. Many XA derivatives include a standard XA Timer 2, and standard UARTs. These blocks have been removed in order to provide other functions on the XA-SCC. There is no Timer 2, and the UARTs have been replaced with full function SCCs.

Watchdog Timer

This timer is a standard XA-G3 Watchdog Timer. See the G3 datasheet in IC25. Also, if you intend to use the Watchdog Timer to assert the $\overline{\text{ResetOut}}$ pin, see $\overline{\text{ResetOut}}$ in the XA-SCC User Manual. The Watchdog Timer is enabled at reset, and must be periodically fed to prevent timeout. If the watchdog times out, it will generate an internal reset; and if $\overline{\text{ResetOut}}$ is enabled the internal reset will generate a $\overline{\text{ResetOut}}$ pulse (active low pulse on $\overline{\text{ResetOut}}$ pin.)

Reset

On the XA-SCC there are two pins associated with reset. The $\overline{\text{ResetIn}}$ pin provides an external reset into the XA-SCC. The port pin P3.2_Timer0_$\overline{\text{ResetOut}}$ output can be configured as $\overline{\text{ResetOut}}$.

Because $\overline{\text{ResetOut}}$ does not reflect $\overline{\text{ResetIn}}$, the $\overline{\text{ResetOut}}$ pin can be tied directly back into the $\overline{\text{ResetIn}}$ pin without other PC board logic. This configuration will make all resets (internal or external) appear to the XA as external resets. See the XA-SCC User Manual for a full discussion of the reset functions.

ResetIn

The ResetIn function is the standard XA-G3 ResetIn function. The $\overline{\text{ResetIn}}$ signal does NOT get passed on to $\overline{\text{ResetOut}}$. See the XA-SCC User Manual for details on reset.

ResetOut

The P3.2_Timer0_$\overline{\text{ResetOut}}$ pin provides an external indication (if the $\overline{\text{ResetOut}}$ function is enabled in the RSRSRC register) via an active low output when an internal reset occurs (internal reset is Reset instruction or Watchdog time out.) If the $\overline{\text{ResetOut}}$ function is enabled, the $\overline{\text{ResetOut}}$ pin will be driven low when a Watchdog reset occurs or the Reset instruction is executed. This signal may be used to inform other devices in the system that the XA-SCC has been internally reset. The $\overline{\text{ResetIn}}$ signal does NOT get passed on to $\overline{\text{ResetOut}}$. When activated, the duration of the $\overline{\text{ResetOut}}$ pulse is 256 system clocks.

WARNING: At power on time, from the time that power coming up is valid, the P3.2_Timer0_$\overline{\text{ResetOut}}$ pin may be driven low for any period from zero nanoseconds up to 258 system clocks. This is true independently of whether $\overline{\text{ResetIn}}$ is active or not.

Reset Source Register

The reset source identification register (RSTSRC) indicates the cause of the most recent XA reset. The cause may have been an externally applied reset signal, execution of the RESET instruction, or a Watchdog reset. Figure 2 shows the fields in the RSTSRC register. If the $\overline{\text{ResetOut}}$ function is tied back into the $\overline{\text{ResetIn}}$ pin, then all resets will be external resets, and will thus appear as external resets in the reset source register. RSTSRC[7] enables the $\overline{\text{ResetOut}}$ function; 1 = Enabled, 0 = Disabled. See XA-SCC User Manual for details; RSTSRC[7] differs in function from most other XA derivatives.

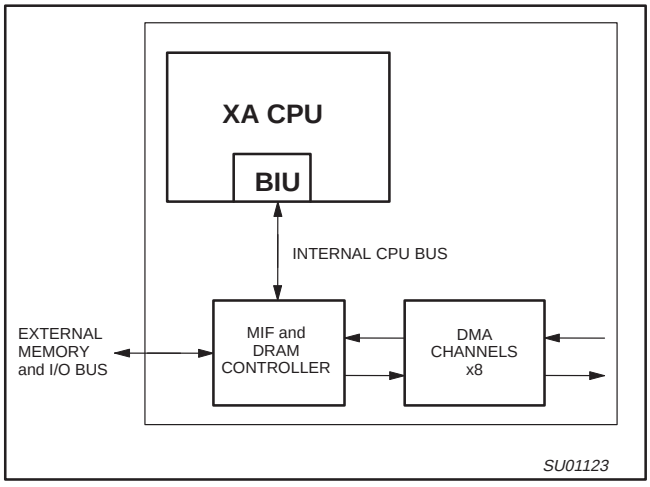


Figure 2. XA CPU Core BIU (Bus Interface Unit)

RSTRC Reg Type and Address = SFR 463h — Reset Value = see below

Not Bit Addressable

	MSB							LSB
	ROEN	—	—	—	—	**R_WD**	**R_CMD**	**R_EXT**
Bit:	7	6	5	4	3	2	1	0

Bit	Symbol	Function
RSTSRC.7	**ROEN**	ResetOut function enable bit – see XA–SCC User Manual for details
RSTSRC.6	**–**	Reserved for future use. Should not be set to 1 by user programs.
RSTSRC.5	**–**	Reserved for future use. Should not be set to 1 by user programs.
RSTSRC.4	**–**	Reserved for future use. Should not be set to 1 by user programs.
RSTSRC.3	**–**	Reserved for future use. Should not be set to 1 by user programs.
RSTSRC.2	**R_WD**	Indicates that the last reset was caused by a watchdog timer overflow (see WARNING.)
RSTSRC.1	**R_CMD**	Indicates that the last reset was caused by execution of the RESET instruction (see WARNING.)
RSTSRC.0	**R_EXT**	Indicates that the last reset was caused by the external $\overline{\text{ResetIn}}$ input.

WARNING:
If $\overline{\text{ResetOut}}$ function is tied back into $\overline{\text{ResetIn}}$ pin, RSTSRC will always show external reset ONLY, because external reset always takes precedence over internal reset.

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Figure 3. RSTSRC Reset Source Register

DRAM Controller and Memory/IO Bus Interface (MIF)

In the memory or system bus interface terminology, generic bus cycles are synonymous with SRAM bus cycles, because these cycles are designed to service SRAMs, Flash, EEPROM, peripheral chips, etc. Chip select output pins function as either $\overline{\text{CS}}$ or $\overline{\text{RAS}}$ depending on whether the memory bank has been programmed as generic or DRAM.

The XA-SCC has a highly programmable memory bus interface with a complete onboard DRAM controller. Most DRAMs (up to 8MBytes per $\overline{\text{RAS}}$ pin), SRAMs, Flash, ROMs, and peripheral chips can be connected to this interface with zero glue chips. The bus interface provides 6 mappable chip select outputs, five of which can be programmed to function as $\overline{\text{RAS}}$ strobes to DRAM. $\overline{\text{CAS}}$ generation, proper address multiplexing for a wide range of DRAM sizes, and refresh are all generated onboard. The bus timing for each individual memory bank or peripheral can be programmed to accommodate slow or fast devices.

Each memory bank and it's associated $\overline{\text{RAS}}$ (chip select pin in DRAM mode) output, can be programmed to access up to an 8MByte mappable address space in either EDO or FPM DRAM modes (up to a total of 16MB of DRAM, or 32MB if 16MB of data space and 16MB code space is elected. **WARNING:** Future XA-SCC derivatives may not support separate code and data spaces.)

Each memory bank and associated chip select programmed for "generic" (SRAM, Flash, ROM, peripheral chips, etc) is capable of supporting a 1Mbyte address space (six chip selects can thus support 6MB of SRAM and other generic devices.)

The Memory Interface can be programmed to support both Intel style and 68000 bus style SRAMs and peripherals.

Bus Interface Pins

For this discussion, see Figure 4.

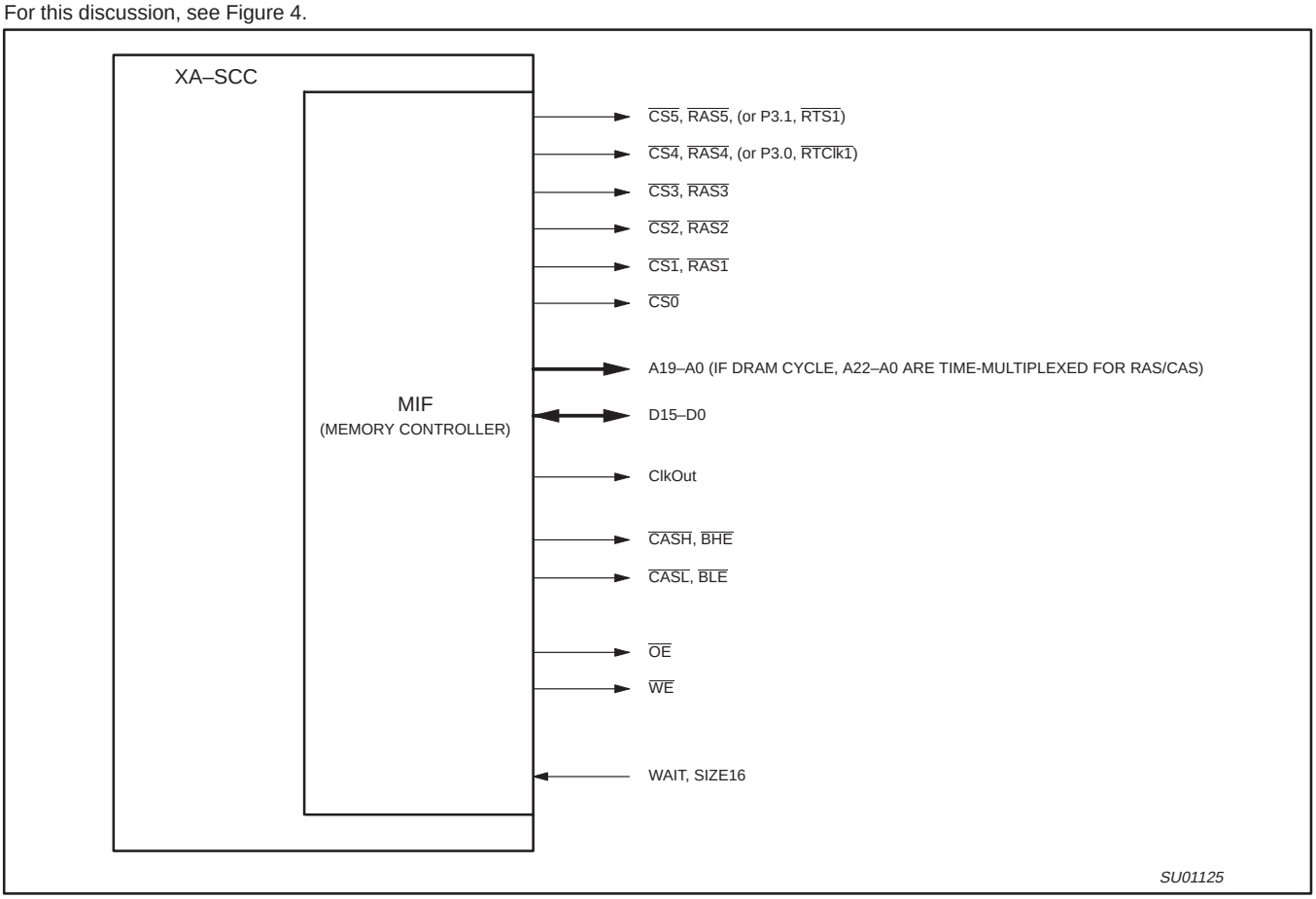


Figure 4. Memory Bus Interface Signal Pins

Chip Selects and RAS pins

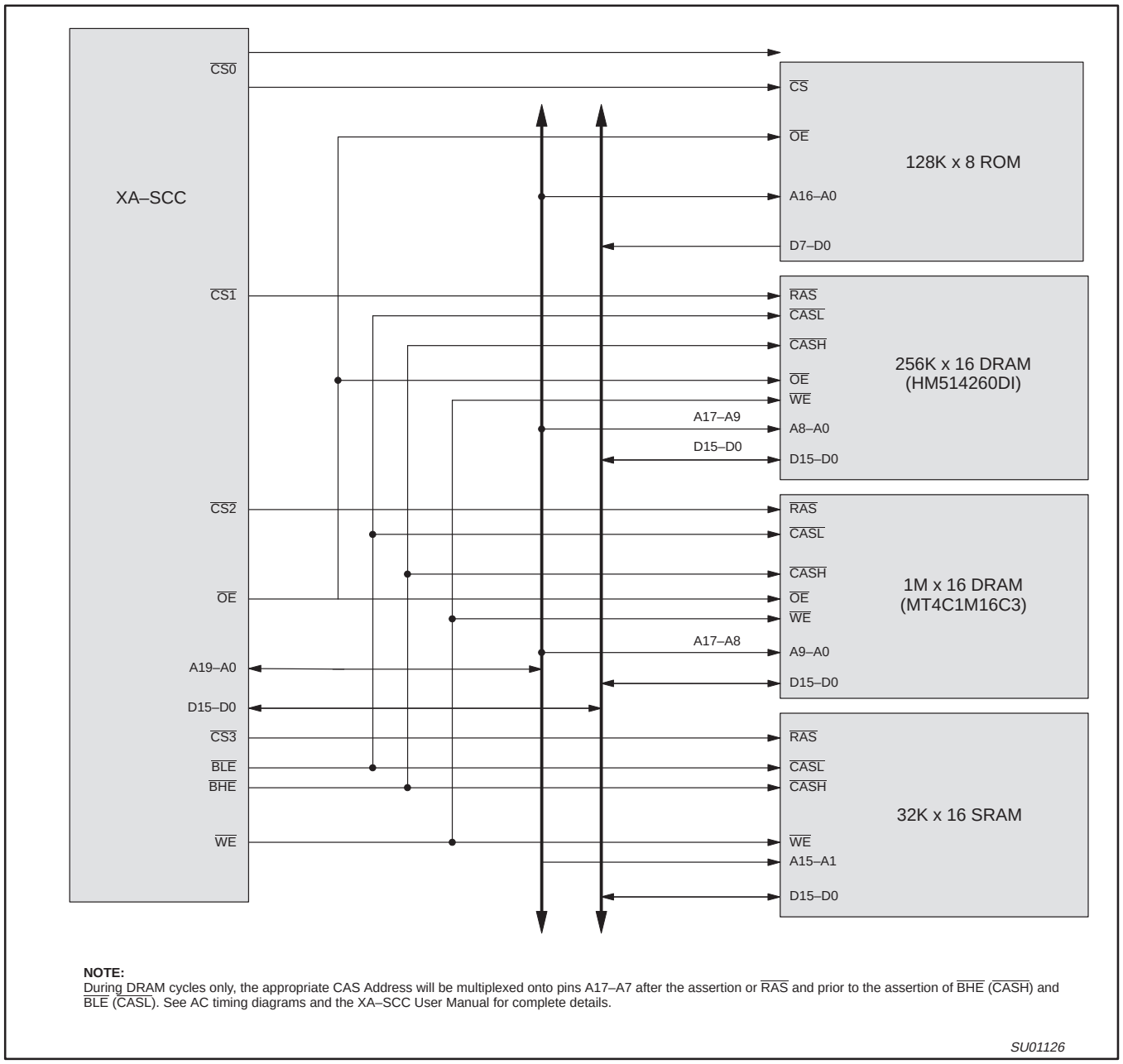
There are six chip select pins ($\overline{CS5}$–$\overline{CS0}$) mapped to six sets of bank control registers. The following attributes are individually programmable for each bank and associated chip select (or $\overline{RAS}$ if DRAM): bank on/off, address range, external device access time, detailed bus strobe sequence, DRAM cycle or generic bus cycle, DRAM size if DRAM, and bus width. Pin $\overline{CS0}$ is always generic in order to service the boot device, thus $\overline{CS0}$ cannot be connected to DRAM.

WARNING: On the external bus, **ALL** XA-SCC reads are 16 bit Reads. If the CPU instruction only specifies 8 bits, then the CPU uses the appropriate byte, and discards the extra byte. Thus “8 Bit Reads” appear to be identical on the bus. **On an 8 bit bus, this will appear as two consecutive 8 bit reads** even though the CPU instruction specified a byte read

Some 8 bit I/O devices (especially FIFOs) cannot operate correctly with 2 bytes being Read for a 1 Byte Read. The most common (and least expensive) solution is to operate these 8 bit devices on a 16 bit bus, and access them in software on all odd byte (or all even byte) boundaries. An added benefit of this technique is that byte reads are faster than on an 8 bit bus, because only 1 word is fetched (a single read) instead of 2 consecutive bytes.

Clock Output

The CLKOUT pin allows easier external bus interfacing in some situations. This output reflects the XTALIn clock input to the XA (referred to internally as CClk or System Clock), but is delayed to match the external bus outputs and strobes. The default is for CLKOUT to be output enabled at reset, but it may be turned off (tri-state disabled) by software via the MICFG MMR.
WARNING: The capacitive loading on this output must not exceed 40pf.



NOTE:
During DRAM cycles only, the appropriate CAS Address will be multiplexed onto pins A17–A7 after the assertion or $\overline{RAS}$ and prior to the assertion of $\overline{BHE}$ ($\overline{CASH}$) and $\overline{BLE}$ ($\overline{CASL}$). See AC timing diagrams and the XA–SCC User Manual for complete details.

SU01126

Figure 5. Typical System Bus Configuration

Table 3. Memory Interface Control Registers

	Register Name	Reg Type	Description
MRBH	"MMR Base Address" High	SFR 8 bits	This SFR is used to relocate the MMRs. It contains address bits a23–a16 of the base address for the 4 KByte Memory Mapped Register space. See XA-SCC User Manual for using this SFR to relocate the MMRs.
MRBL	"MMR Base Address" Low	SFR 8 bits	Contains address bits a15–a12 of the base address for the 4 KByte Memory Mapped Register space.
MICFG	MIF Configuration	MMR 8 bits	Contains the CLKOUT Enable bit.
MBCL	Memory Bank Configuration Lock	MMR 8 bits	Contains the bits for locking and unlocking the BiCFG Registers.
BiCFG	Bank i Configuration	MMR 8 bits	Contains the size, type, bus width, and enable bits for Memory Bank i.
BiAM	Bank i Base Address/DRAM Address Multiplexer Control	MMR 8 bits	Contains the base address bits and DRAM address multiplex control bits for Memory Bank i.
BiTMG	Bank i Timing	MMR 8 bits	Contains the timing control bits for Memory Bank i.
RFSH	Refresh Timing	MMR 8 bits	Contains the refresh time constant and DRAM Refresh Timer enable bit.

Eight Channel DMA Controller

The XA-SCC has eight DMA channels; one Rx DMA channel dedicated to each SCC Receive (Rx) channel, and one Tx DMA channel dedicated to each SCC Transmit (Tx) channel. All DMA channels are optimized to support memory efficient circular data buffers in external memory. All DMA channels can also support traditional linear data buffers.

Transmit DMA Channel Modes

The four Tx channels have four DMA modes specifically designed for various applications of the attached SCCs. These modes are summarized in the following table. Full details for all DMA functions can be found in the DMA chapter of the XA-SCC User Manual.

Table 4. Tx DMA Modes Summary

Mode	Byte Count Source	Maskable Interrupt	Description
Non-SDLC/HDLC Tx Chaining	Header in memory	On stop	DMA channel picks up header from memory at end of transmission. If byte count in header is greater than zero, then DMA transmits the number of bytes specified in the byte count. If byte count equals 0, then a maskable interrupt is generated. This process repeats until byte count in data header is zero. See XA-SCC User manual for details.
SDLC/HDLC Tx Chaining	Header in memory	End of packet (not end of fragment)	Same as above, except DMA header distinguishes between fragment of packet and full pack. See XA-SCC User manual for details.
Stop on TC	Processor loads Byte Count Register (for each fragment)	Byte count completed (Tx DMA stops)	Processor loads byte count into DMA. DMA sends that number of bytes, generates maskable interrupt, and stops.
Periodic Interrupt	Processor loads Byte Count Register (only once)	Each time byte count completed (Tx DMA continues)	DMA runs until commanded to stop by processor. Everytime byte counter rolls over, a new maskable interrupt is generated.

Receive DMA Channel Modes

The Rx DMA channels have four DMA modes specifically designed for various applications of the attached SCCs. These modes are summarized in the following table. For full details on implementation and use, see the XA-SCC User Manual.

Table 5. Rx DMA Modes Summary

Mode	Byte Count Source	Maskable Interrupt	Description
SDLC/HDLC Rx Chaining	DMA stores byte count in header in memory with data packet.	At end of received packet	When a complete or aborted SDLC/HDLC packet has been received, the packet byte count and status information are stored in memory with the packet. A maskable interrupt is generated.
Periodic Interrupt	Loaded by processor into DMA, used only to determine the number of bytes between interrupts. Processor can infer the byte count from the DMA address pointer.	When Byte Counter reaches zero and is reloaded by DMA hardware from the byte count register.	The DMA channel runs until commanded to stop by the processor. It generates a maskable interrupt once per n bytes, where n is the number written once into the byte count register by the processor, thus an interrupt is generated once every n received bytes.
Asynchronous Character Time Out	Byte Count can be calculated by software from the DMA address pointer.	If no character is received within a specified time out period, then interrupt.	Processor specifies time out period between incoming characters. If no character is received within that time, interrupt is generated.
Asynchronous Character Match	Byte Count can be calculated by software from the DMA address pointer.	When matched character is stored in memory.	There are four match registers, each incoming character is compared to all four registers. When a matched character is stored in memory by DMA, a maskable interrupt is generated.

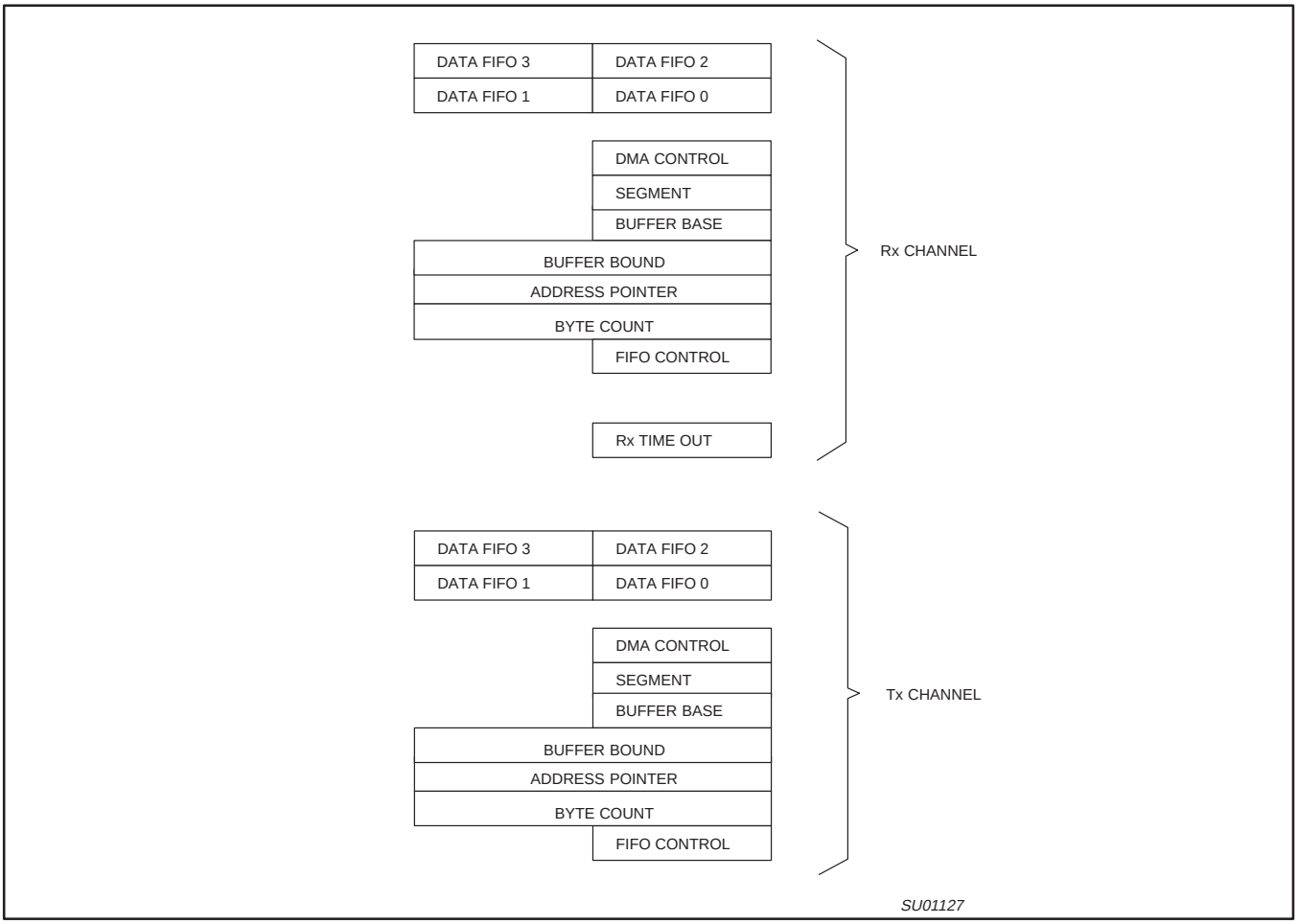


Figure 6. Rx and Tx DMA Registers

DMA Registers

In addition to the 16-bit Global DMA Interrupt Register (which is shared by all eight DMA channels), each DMA channel has seven control registers and a four-byte Data FIFO. The four Rx DMA channels have one additional register, the Rx Character Time Out Register. All DMA registers can be read and written in Memory Mapped Register (MMR) space. These registers are summarized below.

- Global DMA Interrupt Register (not shown in figure): All DMA interrupt flags are in this register .
- DMA Control Register: Contains the master mode select and interrupt enable bits for the channel.
- Segment Register: Holds A23–A16 (the current segment) of the 24-bit data buffer address.
- Buffer Base Register: Holds a pointer (A15–A8) to the lowest byte in the memory buffer.
- Buffer Bound Register: Points to the first out-of-bounds address above a circular buffer.
- Address Pointer Register: Points to a single byte or word in the data buffer in memory. The 24-bit DMA address is formed by concatenating the contents of the Segment Register [A23–A16] with the contents of the Address Pointer Register [A15–A0].
- Byte Count Register: Holds the initial number of bytes to be transferred. In Tx Chaining mode, this register is not used because the byte count is brought into the byte counter from buffer headers in memory.
- FIFO Control & Status Register: Holds the queuing order and full/empty status for the Data FIFO Registers.
- Data FIFO Registers: A four-byte data FIFO buffer internal to the DMA channel.
- Rx Char Time Out Register (RxCTOR, Rx DMA channels only): Holds the initial value for an 8-bit character timeout countdown timer which can generate an interrupt.

Quad Serial Communications Controllers with Autobaud

- Asynchronous features:
  - Asynchronous transfers up to 921.6Kbps
  - Can monitor input stream for up to four match characters per receiver
  - 5, 6, 7, or 8 data bits per character.
  - 1, 1.5, or 2 Stop bits per character.
  - Even or Odd parity generate and check.
  - Parity, Rx Overrun, and Framing Error detection.
  - Break detection.
  - Supports hardware Autobaud detection and response up to 921.6Kbps.
- SDLC/HDLC features:
  - Automatic Flag and Abort Character generation and recognition.
  - Automatic CRC generation and checking (can be disabled for “pass-thru.”)
  - Automatic zero-bit insertion and stripping.
  - Automatic partial byte residue code generation.
  - 14-bit Packet byte count stored in memory with received packet by DMA.
- Synchronous character oriented protocol features:
  - Automatic CRC generation and checking.
  - One (Monosync) or two (Bisync) sync characters option.
  - External Sync option.
- Transparent mode for bit-streaming applications.
- Data encoding/decoding options:
  - FM0 (Biphase Space)
  - FM1 (Biphase Mark)
  - NRZ
  - NRZI
- Programmable Baud Rate Generator, and 7/8 Clock Prescaler option.
- Auto Echo and Local Loopback modes.
- Supports hardware V.54/2047 generation and checking.
- IDL (2B + D) supported on three SCC channels. Supports both “8 bit” and “10 bit” IDL.

IDL Time Division Multiplexor

SCC0, SCC1, and SCC2 can be internally connected to the on-chip IDL Interface, a glueless industry standard interface to Layer One devices such as U-Chips or S/T chips. Thus connected, the three SCCs can efficiently support the ISDN B1, B2, and D channels, while the IDL Interface time-multiplexes and demultiplexes the outgoing and incoming serial data streams.

If software enables the IDL interface, then SCC0 is connected to IDL. Optionally, the software can also connect SCC1 and SCC2 to the IDL interface. SCC3 cannot be connected to the IDL interface. See the IDL chapter in the XA-SCC User Manual.

In Figure 7, SCC0 is connected to IDL because IDL has been enabled by software. Software, in this example has also connected SCC1 to IDL, and has bypassed IDL for SCC2. SCC3 cannot be connected to IDL. If there are pins not being used by any of the SCCs, software can assign alternate functions to those pins; see the pin steering logic in the “Pins” appendix of the XA-SCC User Manual. For complete documentation on the IDL interface, see the IDL chapter in the XA-SCC User Manual.

SCP Serial Interface Controller

The SCP Interface provides a full duplex, industry standard synchronous serial communication bus, similar to SPI and Microwire. SCP can be used to transfer control and status information to other chips, and for accessing serial flash devices. See the IDL interface chapter in the XA-SCC User Manual.

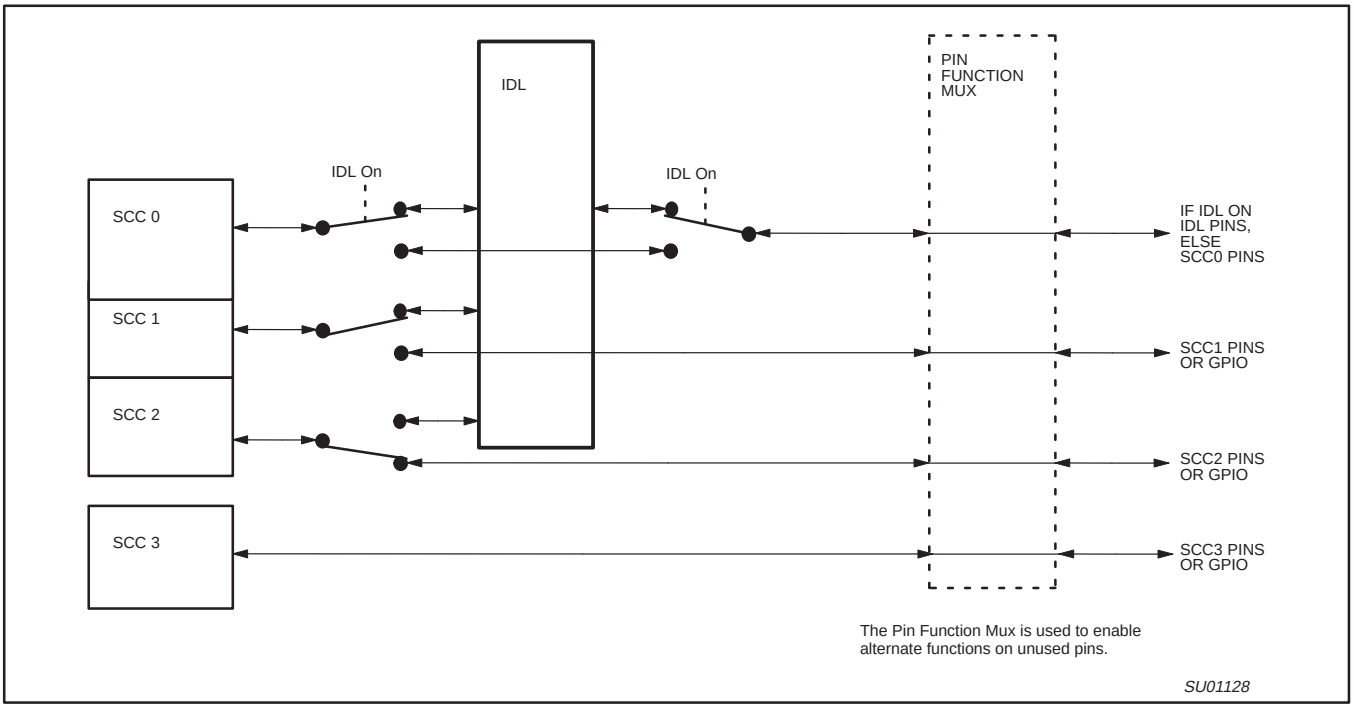


Figure 7. IDL Connection Options

Dual v.54 and 2047 Generators/Checkers

One of the two hardware generator/checkers which support the V.54/2047 line testing standards can be attached to each SCC. During V.54/2047 line testing sequences, the V.54/2047 units can be programmed to generate an interrupt when certain error criteria have been detected on the transmissions lines. The CPU can determine the quality of the transmission line by reading the V.54/2047 units' status registers.

Autobaud Detectors

Each SCC has it's own Autobaud detector, capable of baud rate detection up to 921.6Kbaud. The detectors can be programmed to automatically echo the industry standard autobaud sequences. They can be programmed to update the necessary control registers in the SCCs, and turn on the receiver; which in turn will automatically initiate DMA into memory of received data. Thus, once the baud rate is determined, reception begins without intervention from the processor. When the baud rate is detected, a maskable interrupt is sent to the processor. See the Autobaud chapter in the XA-SCC User Manual for details.

I/O PORT OUTPUT CONFIGURATION

Port input/output configurations are the same as standard XA ports: open drain, quasi-bidirectional, push-pull, and off (off means tri-state Hi-Z, and allows the pin to be used as an input. **WARNING:** At power on time, from the time that power coming up is valid, the P3.2_Timer0_$\overline{\text{ResetOut}}$ pin may be driven low for any period from zero nanoseconds up to 258 system clocks. This is true independently of whether $\overline{\text{ResetIn}}$ is active or not.

POWER REDUCTION MODES

The XA-SCC supports Idle and Power Down modes of power reduction. The idle mode leaves most peripherals running in order to allow them to activate the processor when an interrupt is generated.

The power down mode stops the oscillator in order to absolutely minimize power. The processor can be made to exit power down mode via a reset or one of the external interrupt inputs (INT0 or INT1). This will occur if the interrupt is enabled and its priority is higher than that defined by IM3 through IM0. In power down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM, register, and SFR contents at the point where power down mode was entered. **WARNING:** V_{DD} must be raised to within the operating range before power down mode is exited.

INTERRUPTS

In the XA architecture, all exceptions, including Reset, are handled in the same general exception structure. The highest priority exception is of course Reset, and it is non-maskable. All exceptions are vectored through the Exception Vector Table in low memory. Coming out of Reset, these vectors must be stored in non-volatile memory based at location 000000. Later in the boot sequence, DRAM or SRAM can be mapped into this address space if desired. There is a feature in the XA-SCC Memory Controller called "Bank Swap" that supports replacing the ROM vector table and other low memory with RAM. See the XA-SCC User Manual for details.

The XA-SCC has a standard XA CPU Interrupt Controller, implemented with 15 Maskable Event Interrupts. Event Interrupts are defined as maskable interrupts usually generated by hardware events. However, in the XA-SCC, 4 of the 15 Event Interrupts are generated by software writing directly to the interrupt flag bit. These 4 interrupts are referred to as High Priority Software Interrupts.

See the IC25 XA Data Handbook for a full explanation of the exception structure, including event interrupts, of the XA CPU. Because the High Priority Software Interrupts are specific to the XA-SCC, they are explained in the XA-SCC User Manual.

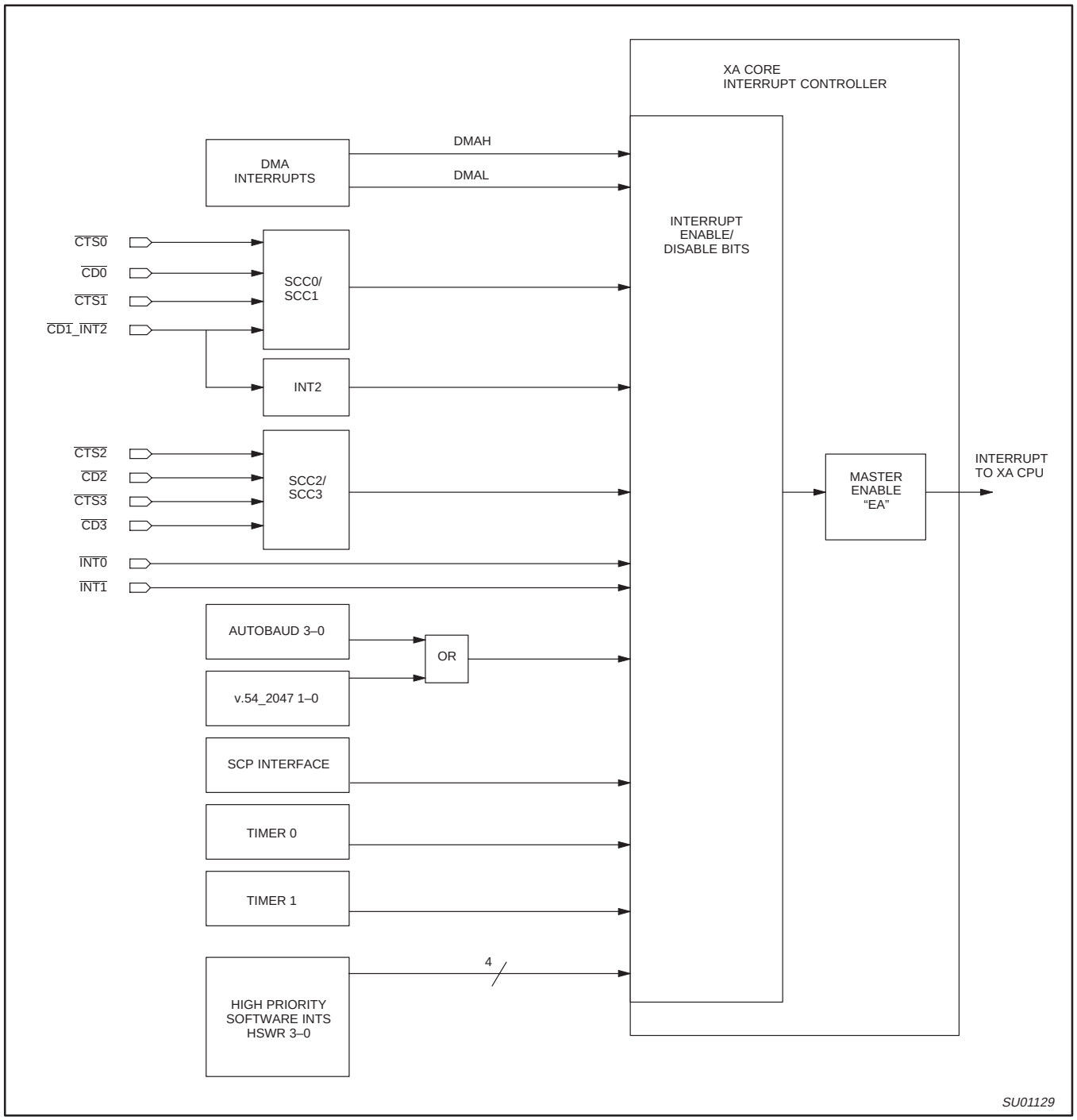


Figure 8. XA-SCC Interrupt Structure Overview

Table 6. SCC0 Interrupts (Interrupt structure is the same except for bit locations for all 4 SCCs)

Potential SCC0 Interrupt	Individual Enable Bit MMR Hex Offset	Source Bit MMR Hex Offset	Group Enable Bit(s) MMR Hex Offset	Group Flag Bit MMR Hex Offset	Master Enable Bit MMR Hex Offset
Rx Character Available	–	RR0[0]	WR1[4:3]	Even Channel Rx IP RR3[5]	SCC0/1 Master Interrupt Enable WR9[3]
SDLC EOF	–	RR1[7]			
CRC/Framing Error	–	RR1[6]			
Rx Overrun	–	RR1[5]			
Parity Error	WR1[2]	RR1[4]			
Tx Buffer Empty	See WR1[1]	RR0[2]	Tx Interrupt Enable WR1[1]	Even Channel Tx IP RR3[4]	
Break/Abort	Break/Abort IE WR15[7]	RR0[7]	Master External/ Status Interrupt Enable WR1[0]	Even Channel External/Status IP RR3[3]	
Tx Underrun/EOM	Tx Underrun/EOM IE WR15[6]	RR0[6]			
CTS	CTS IE WR15[5]	RR0[5]			
SYNC/HUNT	SYNC/HUNT IE WR15[4]	RR0[4]			
DCD	DCD IE WR15[3]	RR0[3]			
Zero Count	Zero Count IE WR15[1]	RR0[1]			

EXCEPTION/TRAPS PRECEDENCE

DESCRIPTION	VECTOR ADDRESS	ARBITRATION RANKING
Reset (h/w, watchdog, s/w)	0000–0003	0 (High)
Breakpoint	0004–0007	1
Trace	0008–000B	1
Stack Overflow	000C–000F	1
Divide by 0	0010–0013	1
User RETI	0014–0017	1
TRAP 0–15 (software)	0040–007F	1

EVENT INTERRUPTS

Description Event Interrupt Source	Flag Bit	Interrupt Vector Address	Enable Bit (SFR)	Priority Register Bit Field (SFR)	Arb. Rank
High Priority Software Interrupt 3	HSWR3 MMR	00BF–00BC	EHSWR3	PHSWR3	17
High Priority Software Interrupt 2	HSWR2 MMR	00BB–00B8	EHSWR2	PHSWR2	16
High Priority Software Interrupt 1	HSWR1 MMR	00B7–00B4	EHSWR1	PHSWR1	15
High Priority Software Interrupt 0	HSWR0 MMR	00B3–00B0	EHSWR0	PHSWR0	14
SCP Port	SPFG SCPCS[3] MMR	00AF–00AC	ESCP	PSCP	13
Autobaud and V.54/2047	multiple OR from Autobauds 3–0 & V.54/2047 A and B	00AB–00A8	EAuto	PAutoB	12
SCC “SCC2/3” Interrupt	multiple OR from SCC2 & SCC3	00A7–00A4	ESC23	PSC23	11
SCC “SCC0/1” Interrupt	multiple OR from SCC0 & SCC1	00A3–00A0	ESC01	PSC01	10
DMA “DMAH” Interrupt	multiple OR from DMA	009B– 0098	EDMAH	PDMAH	8
DMA “DMAL” Interrupt	multiple OR from DMA	0097–0094	EDMAL	PDMAL	7
External Interrupt 2 ($\overline{INT2}$)	IE2 MMR	0093–0090	EX2	PX2	6
Timer 1	TF1 SFR	008F–008C	ET1	PT1	5
External Interrupt 1 ($\overline{INT1}$)	IE1 SFR	008B–0088	EX1	PX1	4
Timer 0	TF0 SFR	0087–0084	ET0	PT0	3
External Interrupt 0 ($\overline{INT0}$)	IE0 SFR	0083–0080	EX0	PX0	2

SOFTWARE INTERRUPTS

DESCRIPTION	FLAG BIT	VECTOR ADDRESS	ENABLE BIT	INTERRUPT PRIORITY
Software Interrupt 1	SWR1	0100–0103	SWE1	(fixed at 1)
Software Interrupt 2	SWR2	0104–0107	SWE2	(fixed at 2)
Software Interrupt 3	SWR3	0108–010B	SWE3	(fixed at 3)
Software Interrupt 4	SWR4	010C–010F	SWE4	(fixed at 4)
Software Interrupt 5	SWR5	0110–0113	SWE5	(fixed at 5)
Software Interrupt 6	SWR6	0114–0117	SWE6	(fixed at 6)
Software Interrupt 7	SWR7	0118–011B	SWE7	(fixed at 7)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on any other pin to V_{SS}	–0.5 to V_{DD}+0.5V	v
Maximum IOL per I/O pin	15	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

PRELIMINARY DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0V ±10% or 3.3V ±10% unless otherwise specified;
Tamb = –40°C to +85°C for industrial, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{DD}	Power supply current, operating	5.0V, 30 MHz		75	120	mA
		3.3V, 30 MHz		63	80	mA
I_{ID}	Power supply current, Idle mode	5.0V, 30 MHz		62	100	mA
		3.3V, 30 MHz		50	65	mA
I_{PDI}	Power supply current, Power Down mode[1]	5.0V, 3.0V			500	µA
V_{RAM}	RAM keep-alive voltage		1.5			V
V_{IL}	Input low voltage		–0.5		$0.22V_{DD}$	V
V_{IH}	Input high voltage, except Xtal1, RST		2.2			V
V_{IH1}	Input high voltage to Xtal1, RST	For both 3.0 & 5.0V	$0.7\ V_{DD}$			V
V_{OL}	Output low voltage all ports[8]	I_{OL} = 3.2mA, V_{DD} = 4.5V			0.5	V
		I_{OL} = 1.0mA, V_{DD} = 3.0V			0.4	V
V_{OH1}	Output high voltage, all ports	I_{OH} = –100µA, V_{DD} = 4.5V	2.4			V
		I_{OH} = –30µA, V_{DD} = 3.0V	2.0			V
V_{OH2}	Output high voltage, all ports	I_{OH} = 3.2mA, V_{DD} = 4.5V	2.4			V
		I_{OH} = 1.0mA, V_{DD} = 3.0V	2.2			V
C_{IO}	Input/Output pin capacitance				15	pF
I_{IL}	Logical 0 input current, all ports[7]	V_{IN} = 0.45V			–50	µA
I_{LI}	Input leakage current, all ports[6]	V_{IN} = V_{IL} or V_{IH}			±10	µA
I_{TL}	Logical 1 to 0 transition current, all ports[5]	At V_{DD} = 5.5V			–650	µA
		At V_{DD} = 3.6V			–250	µA

NOTES:
1. V_{DD} must be raised to within the operating range before power down mode is exited.
2. Ports in quasi-bidirectional mode with weak pullup .
3. Ports in PUSH-PULL mode, both pullup and pulldown assumed to be the same strength.
4. In all output modes.
5. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when V_{IN} is approximately 2V.
6. Measured with port in high impedance mode.
7. Measured with port in quasi-bidirectional mode.
8. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA (*NOTE: This is 85°C specification for V_{DD} = 5V.)
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

PRELIMINARY AC ELECTRICAL CHARACTERISTICS (5.0V ±10%)[1]

V_{DD} = 5.0V ±10%, T_{amb} = –40°C to +85°C (industrial)

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			MIN	MAX	
All Cycles					
F_C		System Clock Frequency	0	30	MHz
t_C	25	System Clock Period = $1/F_C$	33.33	–	ns
t_{CHCX}	25	XTALIN High Time	t_C* 0.5	–	ns
t_{CLCX}	25	XTALIN Low Time	t_C* 0.4	–	ns
t_{CLCH}	25	XTALIN Rise Time	–	5	ns
t_{CHCL}	25	XTALIN Fall Time	–	5	ns
t_{AVSL}	All	Address Valid to Strobe low	t_C – 21	–	ns
t_{CHAH}	All	Address hold after CLKOUT rising edge[9]	1	–	ns
t_{CHAV}	All	Delay from CLKOUT rising edge to address valid	–	25	ns
t_{CHSH}	All	Delay from CLKOUT rising edge to Strobe High[9]	1	21	ns
t_{CHSL}	All	Delay from CLKOUT rising edge to Strobe Low[9]	1	19	ns
t_{CODH}	26	ClkOut Duty Cycle High (into 40pF max.) (See **Warning** Note 5 on page 31.)	t_{CHCX}–7	t_{CHCX}+3	ns
t_{CPWH}	13, 14, 16, 20, 21, 22	CAS Pulse Width High	t_C – 12	–	ns
t_{CPWL}	13, 21	CAS Pulse Width Low	t_C – 10	–	ns
All DRAM cycles					
t_{RP}	24	RAS precharge time, thus minimum $\overline{RAS}$ high time[8]	(n * t_C) –16 note 8	–	ns
Generic Data Read Only					
t_{AHDR}	9, 16	Address hold (A19–A1 only, not A0) after $\overline{CS}$, $\overline{BLE}$, $\overline{BHE}$ rise at end of Generic Data Read Cycle (not code fetch)	t_C –12	–	ns
Data Read and Instruction Fetch Cycles					
t_{DIS}	9, 10, 12–14, 16, 17, 20, 21	Data In Valid setup to ClkOut rising edge	25	–	ns
t_{DIH}		Data In Valid hold after ClkOut rising edge[2]	0	–	ns
t_{OHDE}	10, 12, 13, 16, 20, 21	$\overline{OE}$ high to XA Data Bus Driver Enable	t_C – 14	–	ns
Write Cycles					
t_{CHDV}		Clock High to Data Valid	–	25	ns
t_{DVSL}		Data Valid prior to Strobe Low	t_C – 23	–	ns
t_{SHAH}	11, 16	Minimum Address Hold Time after strobe goes inactive	t_C – 25	–	ns
t_{SHDH}		Data hold after strobes ($\overline{CS}$ and $\overline{BHE}$/$\overline{BLE}$) high	t_C – 25	–	ns
Refresh					
t_{CLRL}	21	$\overline{CAS}$ low to $\overline{RAS}$ low	t_C – 15	–	ns
Wait Input					
t_{WS}	24	WAIT setup (stable high or low) to CLKOUT rising edge	20	–	ns
t_{WH}	24	WAIT hold (stable high or low) after CLKOUT rising edge	0	–	ns

NOTE:
1. See notes after the 3.3V AC timing table.

AC ELECTRICAL CHARACTERISTICS (3.3V ±10%)

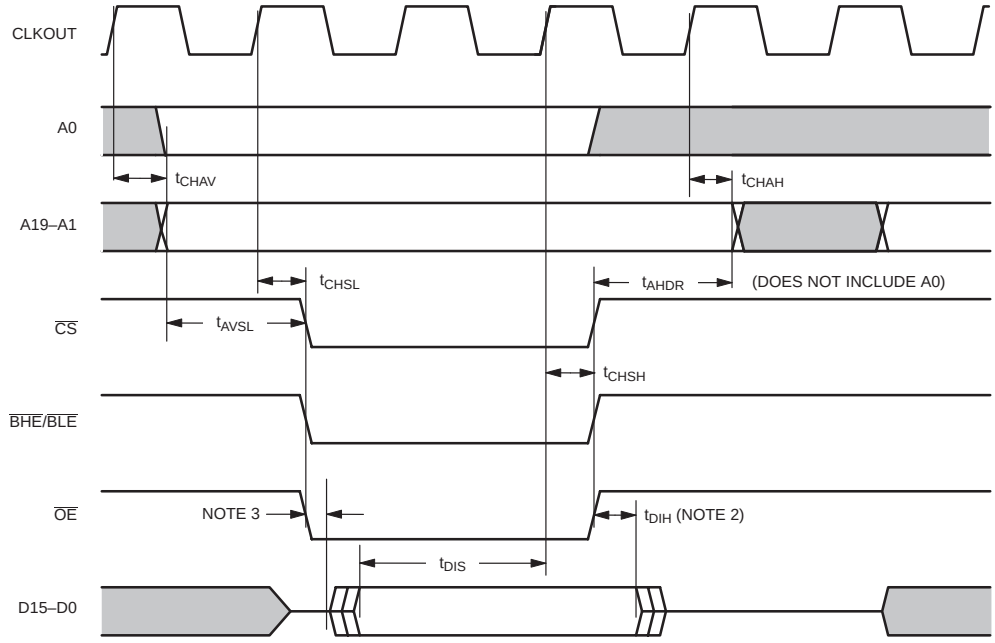
V_{DD} = 3.3V ±10%, T_{amb} = –40°C to +85°C (industrial)

SYMBOL	FIGURE	PARAMETER	LIMITS		UNIT
			MIN	MAX	
All Cycles					
F_C	25	System Clock (internally called CClk) Frequency	0	30	MHz
t_C	25	System Clock Period = 1/FC	33.33	–	ns
t_{CHCX}	25	XTALIN High Time	t_C* 0.5	–	ns
t_{CLCX}	25	XTALIN Low Time	t_C* 0.4	–	ns
t_{CLCH}	25	XTALIN Rise Time	–	5	ns
t_{CHCL}	25	XTALIN Fall Time	–	5	ns
t_{AVSL}	All	Address Valid to Strobe low	t_C – 21	–	ns
t_{CHAH}	All	Address hold after CLKOUT rising edge[9]	1	–	ns
t_{CHAV}	All	Delay from CLKOUT rising edge to address valid	–	30	ns
t_{CHSH}	All	Delay from CLKOUT rising edge to Strobe High[9]	1	28	ns
t_{CHSL}	All	Delay from CLKOUT rising edge to Strobe Low[9]	1	25	ns
t_{CODH}	26	ClkOut Duty Cycle High (into 40pF max.) (See **Warning** Note 5 on page 31.)	t_{CHCX}–7	t_{CHCX}+3	ns
t_{CPWH}	13, 14, 16, 20, 21, 22	CAS Pulse Width High	t_C – 12	–	ns
t_{CPWL}	13, 21	CAS Pulse Width Low	t_C – 10	–	ns
All DRAM cycles					
t_{RP}	24	RAS precharge time, thus minimum $\overline{RAS}$ high time[8]	(n * t_C) –16 note 8	–	ns
Generic Data Read Only					
t_{AHDR}	9, 16	Address hold (A19–A1 only, not A0) after $\overline{CS}$, $\overline{BLE}$, $\overline{BHE}$ rise at end of Generic Data Read Cycle (not code fetch)	t_C –12	–	ns
Data Read and Instruction Fetch Cycles					
t_{DIS}	9, 10, 12–14, 16, 17, 20, 21	Data In Valid setup to ClkOut rising edge	32	–	ns
t_{DIH}		Data In Valid hold after ClkOut rising edge[2]	0	–	ns
t_{OHDE}	10, 12, 13, 16, 20, 21	$\overline{OE}$ high to XA Data Bus Driver Enable	t_C – 19	–	ns
Write Cycles					
t_{CHDV}		Clock High to Data Valid	–	30	ns
t_{DVSL}		Data Valid prior to Strobe Low	t_C – 23	–	ns
t_{SHAH}	11, 16	Minimum Address Hold Time after strobe goes inactive	t_C – 25	–	ns
t_{SHDH}		Data hold after strobes ($\overline{CS}$ and $\overline{BHE}$/$\overline{BLE}$) high	t_C – 25	–	ns
Refresh					
t_{CLRL}	21	$\overline{CAS}$ low to $\overline{RAS}$ low	t_C – 15	–	ns
Wait Input					
t_{WS}	24	WAIT setup (stable high or low) prior to CLKOUT rising edge	25	–	ns
t_{WH}	24	WAIT hold (stable high or low) after CLKOUT rising edge	0	–	ns

NOTES:

1. On a 16 bit bus, if only one byte is being written, then only one of $\overline{BLE}$_$\overline{CASL}$ or $\overline{BHE}$_$\overline{CASH}$ will go active. On an 8 bit bus, $\overline{BLE}$_$\overline{CASL}$ goes active for all (odd or even address) accesses. $\overline{BHE}$_$\overline{CASH}$ will not go active during any accesses on an 8 bit bus.
2. The bus timing is designed to make meeting hold time very straightforward without glue logic. On all generic reads and fetches, in order to meet hold time, the slave device should hold data valid on the bus until the earliest of $\overline{CS}$, $\overline{BHE}$/$\overline{BLE}$, $\overline{OE}$, goes high (inactive), or until the address changes. On all FPM DRAM reads and fetches, hold data valid on the bus until the earliest of $\overline{RAS}$, $\overline{CAS}$, or $\overline{OE}$ goes high (inactive.) On all EDO DRAM reads and fetches, hold data valid on the bus until a new $\overline{CAS}$ is asserted, or until $\overline{OE}$ goes high (inactive.)
3. To avoid tri-state fights during read cycles and fetch cycles, do not drive data bus until $\overline{OE}$ goes active

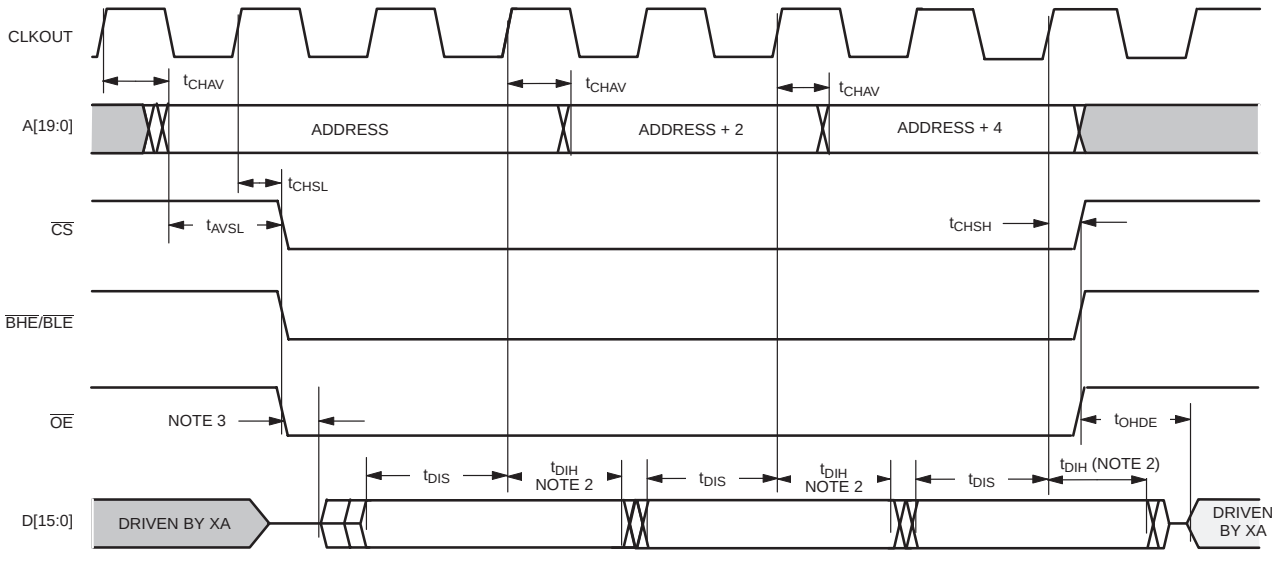
4. To meet hold time, EDO DRAM drives data onto the bus until $\overline{OE}$ rises, or until a new falling edge of $\overline{CAS}$.
5. **WARNING: ClkOut is specified at 40pF max**. More than 40pf on ClkOut may significantly degrade the ClkOut waveform. Load capacitance for all outputs (except ClkOut) = 80pF.
6. Not all combinations of bus timing configuration values result in valid bus cycles. Please refer to the *XA-SCC User Manual* for details.
7. When code is being fetched on the external bus, a burst mode fetch is used. This burst can be from 2 to 16 bytes long. On a 16 bit bus, A3–A1 are incremented for each new word of the burst. On an 8 bit bus, A3–A0 are incremented for each new byte of the burst code fetch.
8. t_{RP} is specified as the minimum high time (thus inactive) on each of the 5 individual $\overline{CS}\_\overline{RAS}$[5:1] pins when such pin is programmed in the memory controller to service DRAM. The number of CClks (system clocks) in t_{RP} is programmable, and is represented by n in the t_{RP} equation in the AC tables. Regardless of what value is programmed into the control register, n will never be less than 2 clocks. Thus at 30MHz system clock, the minimum value for RAS precharge is $t_{RP} = ((2 * t_C) – 16) = ((2 * 33.33) – 16) = 50.6$ns. As the system clock frequency F_C, is slowed down, t_C (system clock period) of course becomes greater, and thus t_{RP} becomes greater.
9. The MIN value for this parameter is guaranteed by design and is not tested in production to the specified limit. In those cases where a maximum value is specified in the table for this parameter, it is tested.



NOTE: On Generic Data Reads, A0 can terminate a full clock period before A19–A1, and therefore should not be used on some peripheral devices.

SU01130

Figure 9. Generic (SRAM, ROM, Flash, IO Devices, etc.) Read on 16 Bit Bus



NOTE: The processor can prefetch from one to eight words.

NOTE 2: To meet the required Data In Hold time, data should be held on the bus at least until the earliest of CS, BHE, BLE, OE goes high, or until the address changes, whichever comes first.

SU01131

Figure 10. Generic Memory (SRAM, ROM, Flash, etc.) Burst Code Fetch on 16 Bit Bus

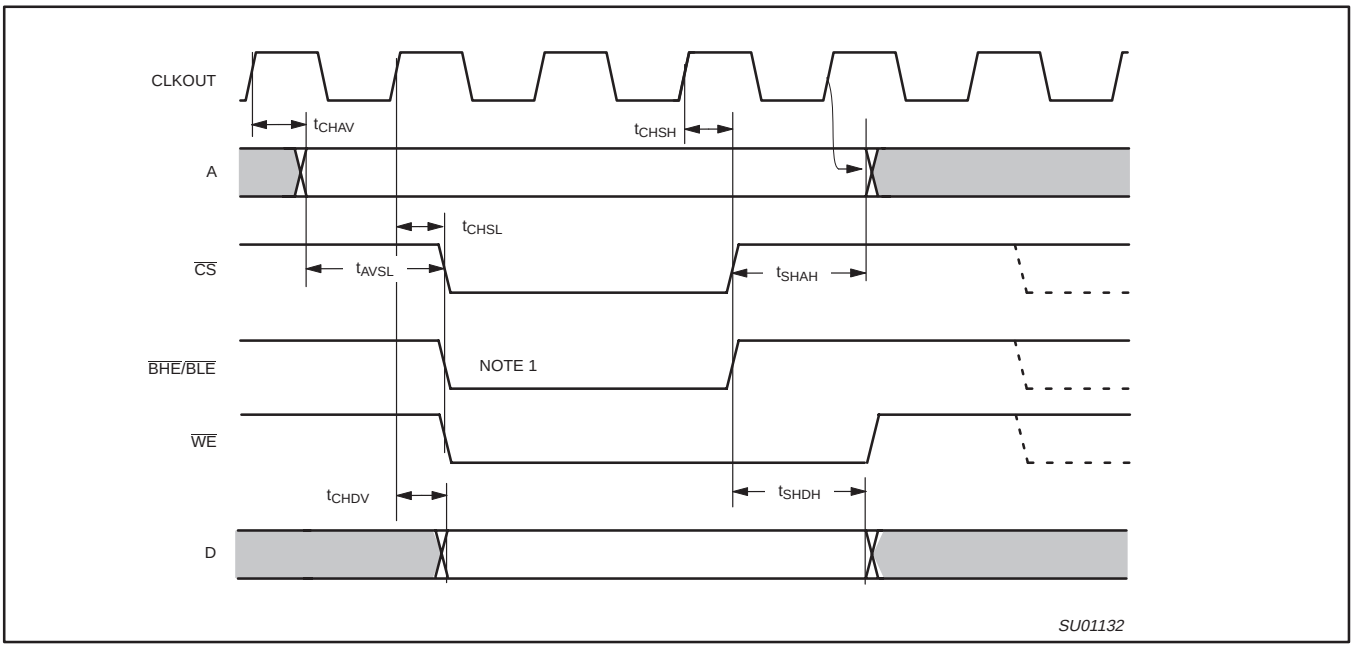


Figure 11. Generic (SRAM, IO Devices, etc.) Write

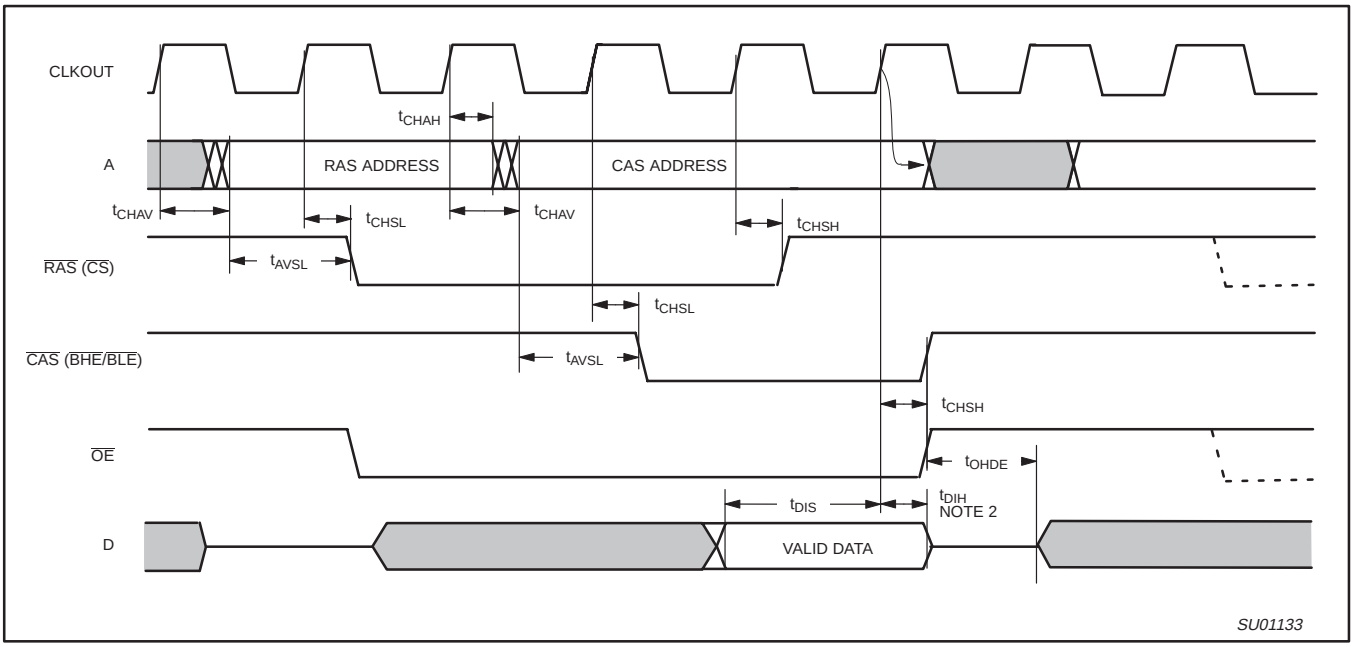
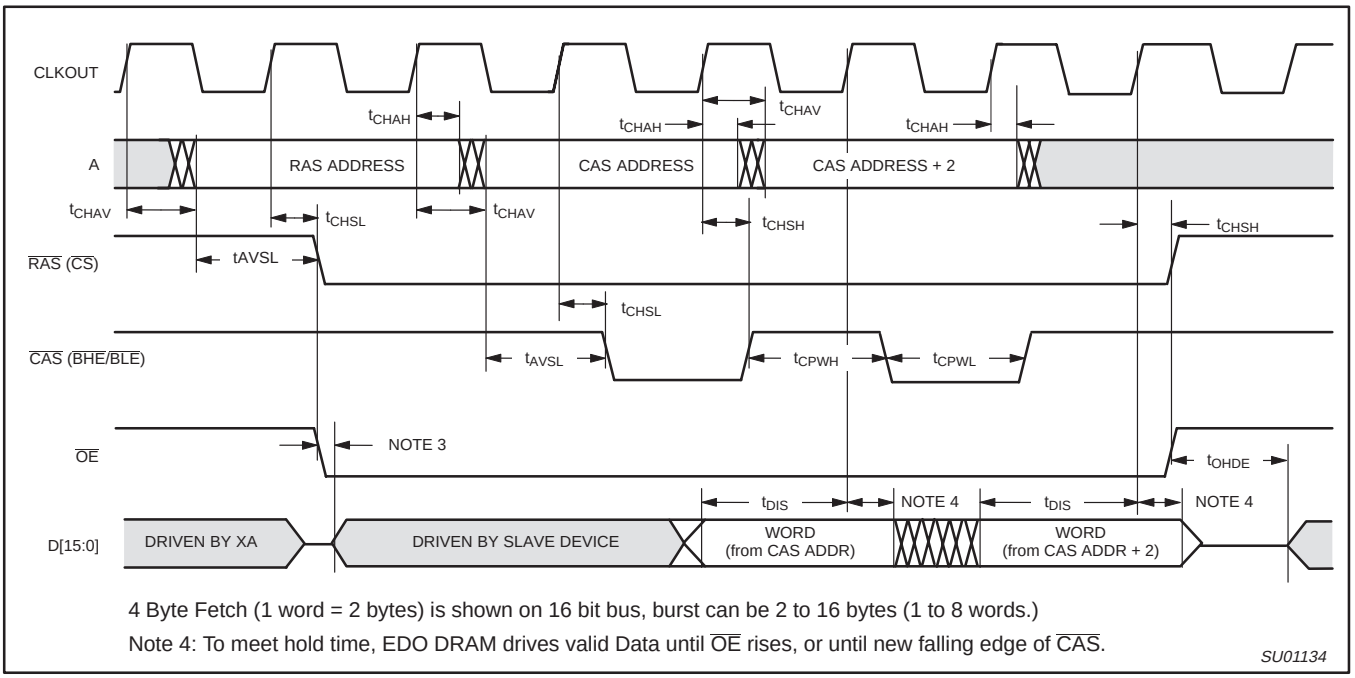


Figure 12. DRAM Single Read Cycle

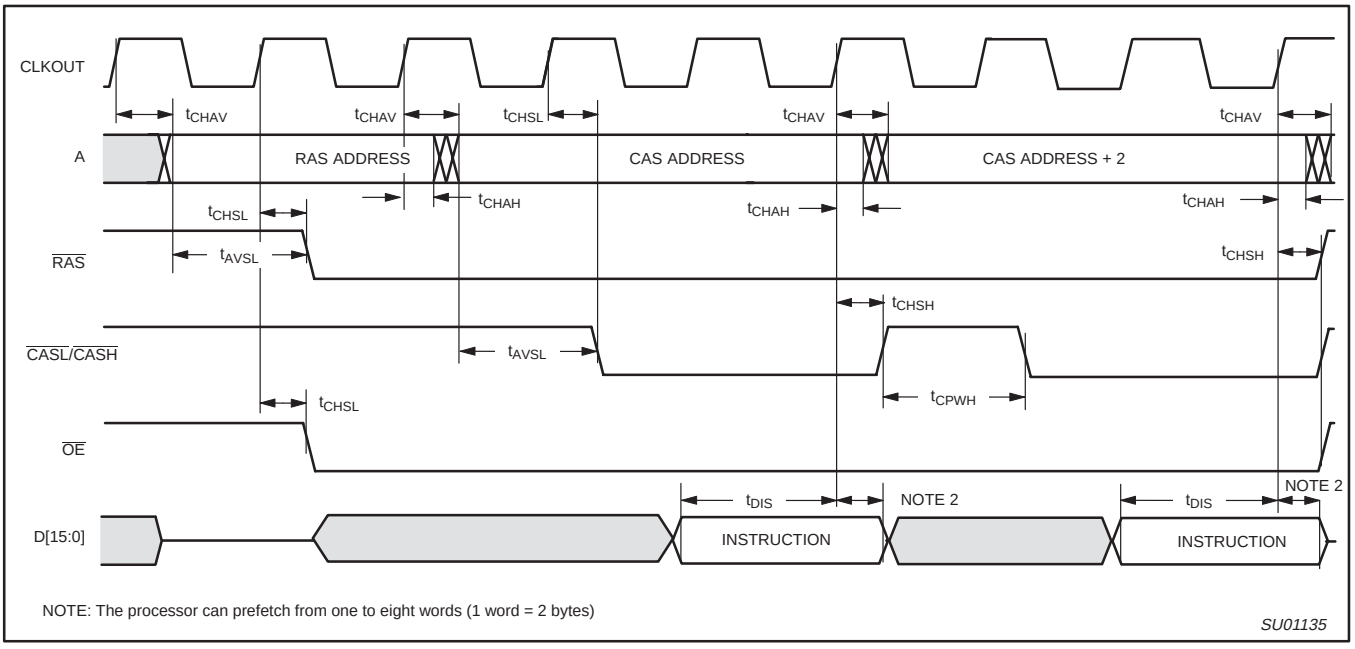


4 Byte Fetch (1 word = 2 bytes) is shown on 16 bit bus, burst can be 2 to 16 bytes (1 to 8 words.)

Note 4: To meet hold time, EDO DRAM drives valid Data until $\overline{OE}$ rises, or until new falling edge of $\overline{CAS}$.

SU01134

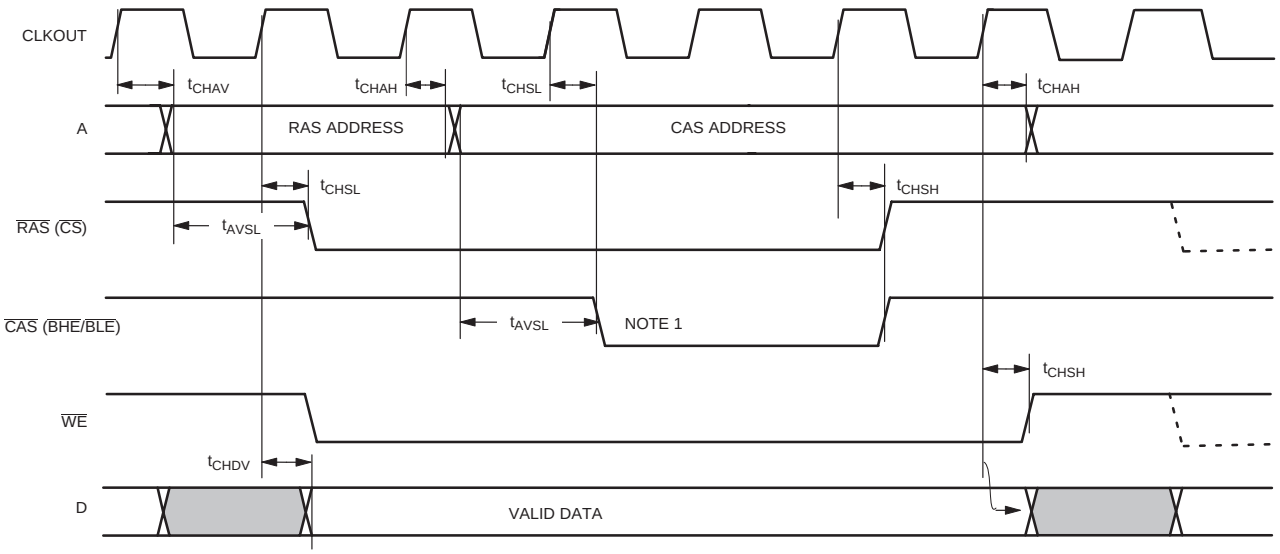
Figure 13. DRAM EDO Burst Code Fetch on 16 Bit Bus



NOTE: The processor can prefetch from one to eight words (1 word = 2 bytes)

SU01135

Figure 14. DRAM FPM (Fast Page Mode) Burst Code Fetch

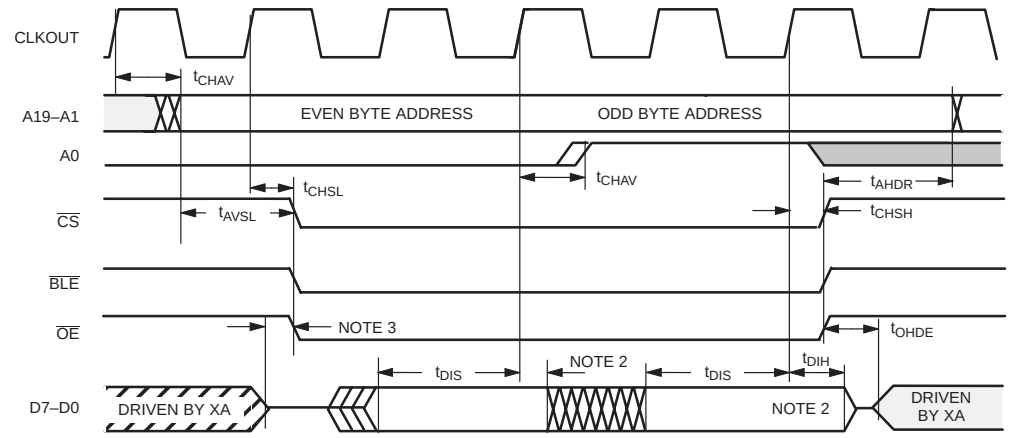


NOTE: If only one byte is being written, then only the corresponding $\overline{CAS}$ signal goes active. On 8 bit bus, $\overline{CASH}$ is inactive, and $\overline{CASL}$ goes active for both even and odd addressed bytes.

: $\overline{OE}$ is inactive during all writes.

SU01136

Figure 15. DRAM Write (on 16 Bit Bus, also 8 Bit Write on 8 Bit Bus)



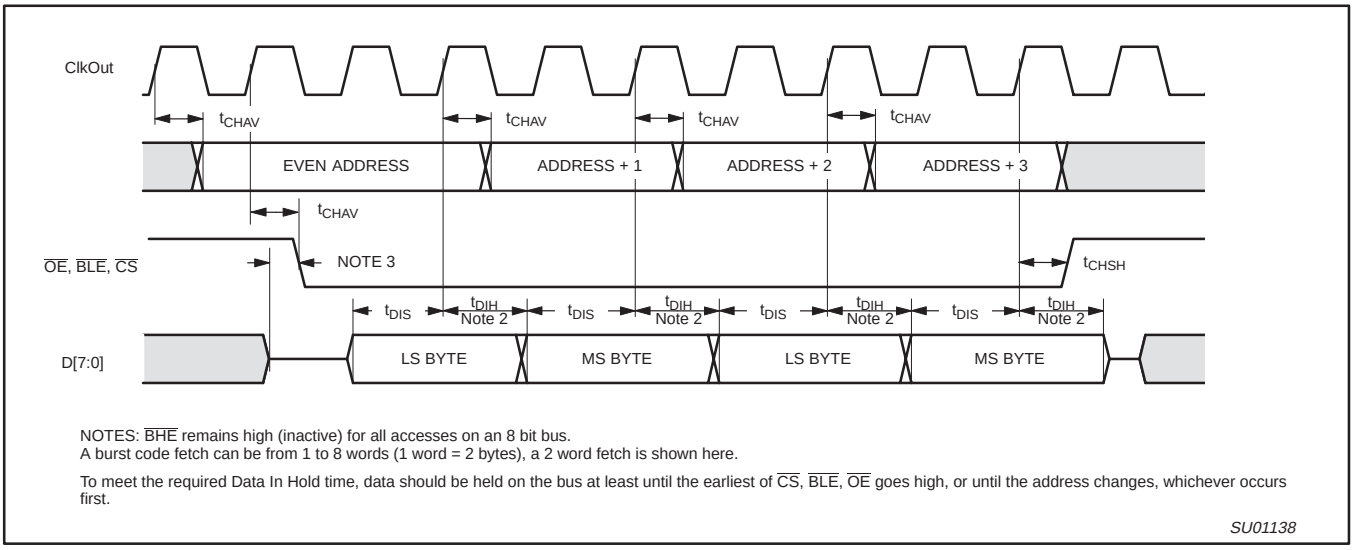
On all cycles on 8 bit bus, $\overline{BHE}$ remains high (inactive).

WARNING: On the external bus, ALL XA–SCC reads are 16 bit Reads. If the CPU instruction only specifies 8 bits, then the CPU uses the appropriate byte, and discards the extra byte. Thus "8 Bit Reads" and "16 bit Reads" appear to be identical on the bus. On an 8 bit bus, this will appear as two consecutive 8 bit reads even though the CPU will only use one of the two bytes.

WARNING: Some 8 bit I/O devices (especially FIFOs) cannot operate correctly with 2 bytes being Read for a 1 Byte Read. The most common (and least expensive) solution is to operate these 8 bit devices on a 16 bit bus, and access them in software on all odd byte (or all even byte) boundaries. An added benefit of this technique is that byte reads are faster than on an 8 bit bus, because only 1 word is fetched (a single read) instead of 2 consecutive bytes.

SU01137

Figure 16. Generic (SRAM, Flash, I/O Device, etc.) Read (16 Bit or 8 Bit) on 8 Bit Bus

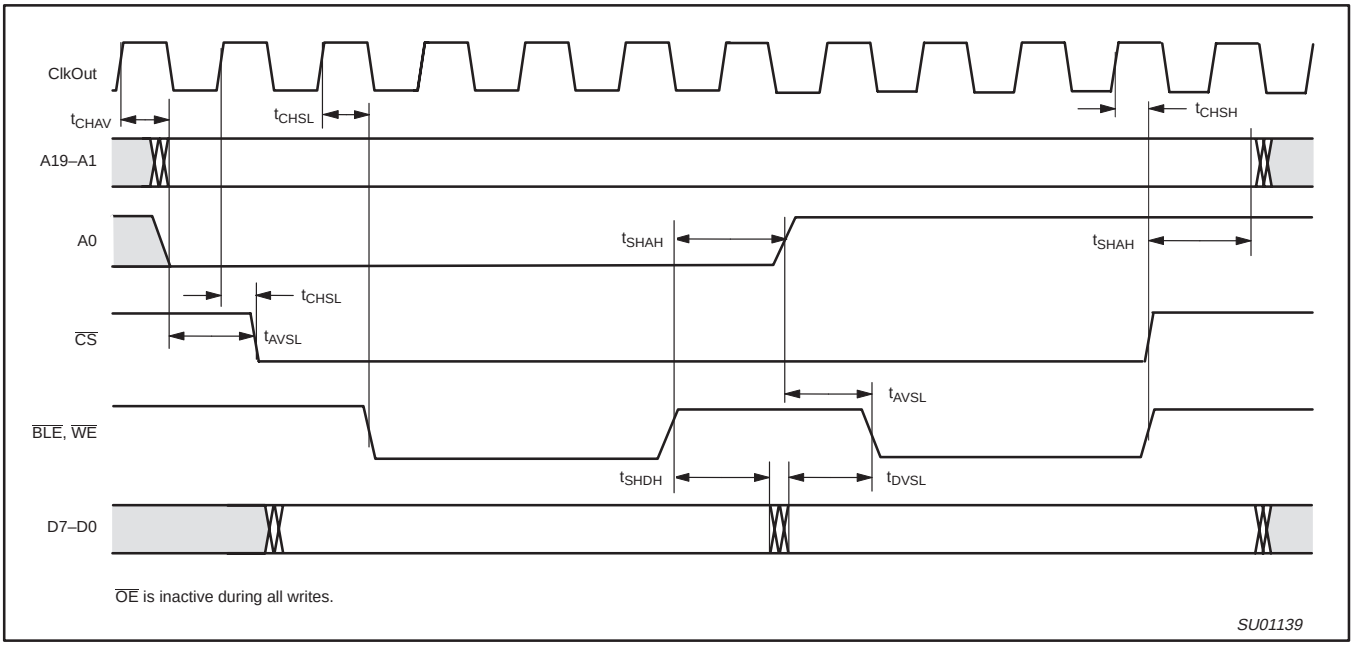


NOTES: $\overline{BHE}$ remains high (inactive) for all accesses on an 8 bit bus.
A burst code fetch can be from 1 to 8 words (1 word = 2 bytes), a 2 word fetch is shown here.

To meet the required Data In Hold time, data should be held on the bus at least until the earliest of $\overline{CS}$, $\overline{BLE}$, $\overline{OE}$ goes high, or until the address changes, whichever occurs first.

SU01138

Figure 17. Burst Code Fetch on 8 bit bus, Generic Memory



$\overline{OE}$ is inactive during all writes.

SU01139

Figure 18. Generic 16 Bit Write on 8 Bit Bus

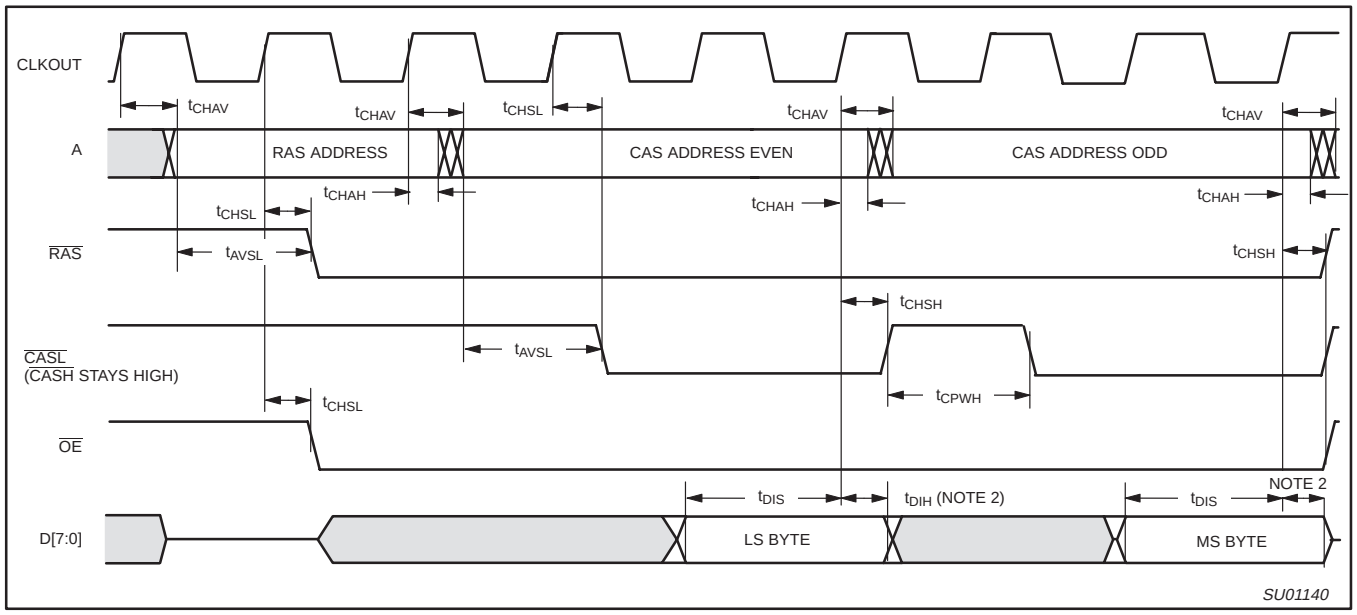


Figure 19. 16 Bit Read on 8 Bit Bus, DRAM (both FPM and EDO)

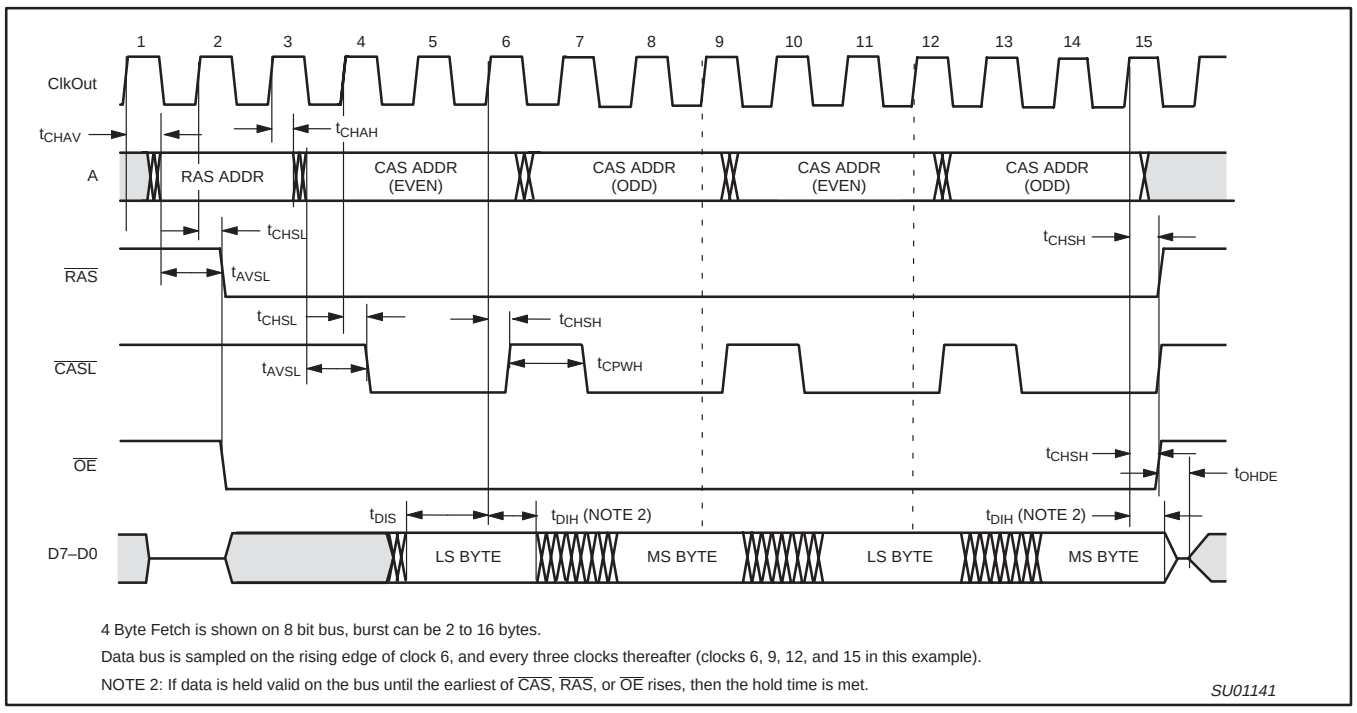


Figure 20. DRAM FPM (Fast Page Mode) Burst Code Fetch on 8 Bit Bus

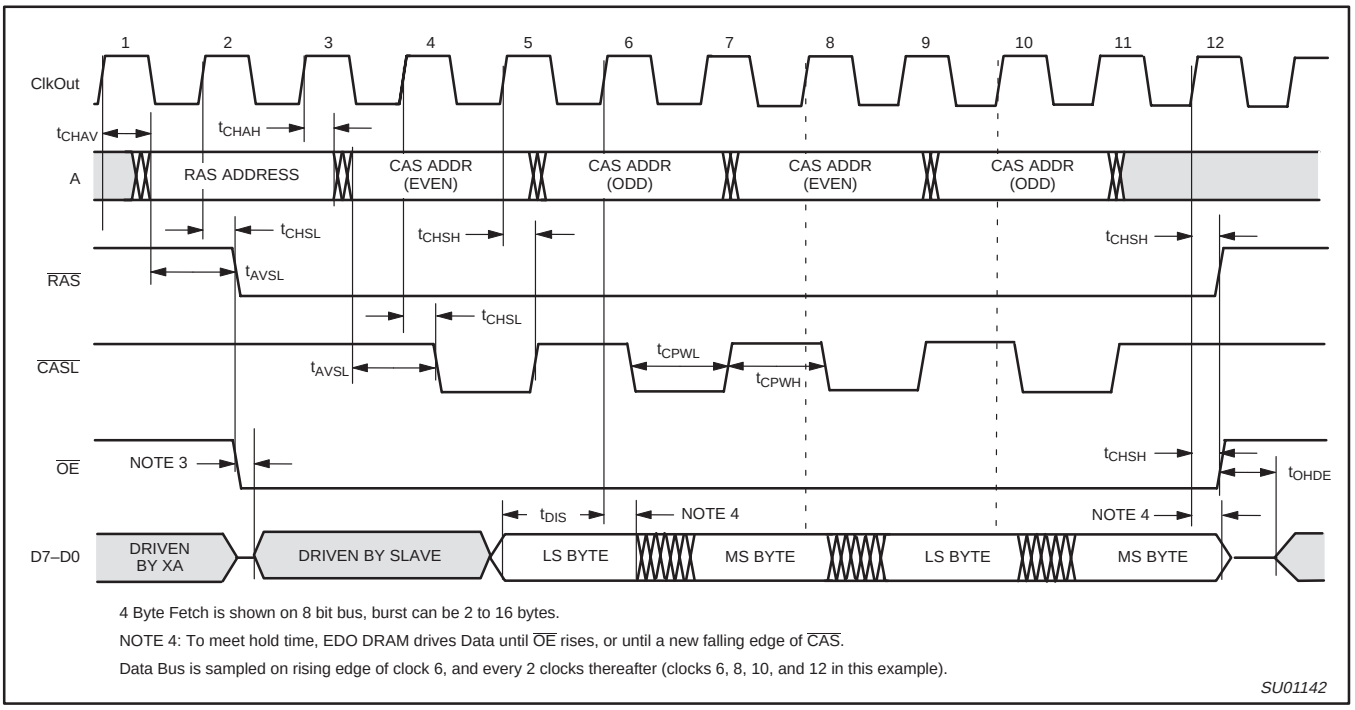


Figure 21. EDO DRAM Burst Code Fetch on 8 Bit Bus

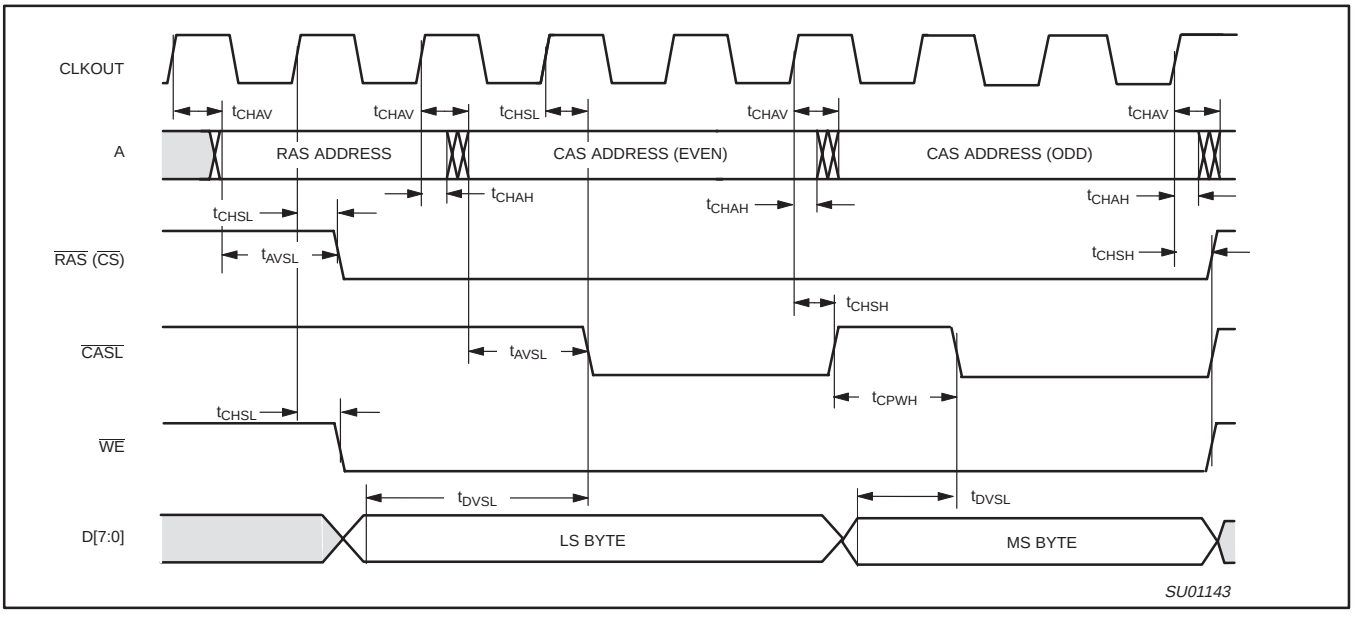
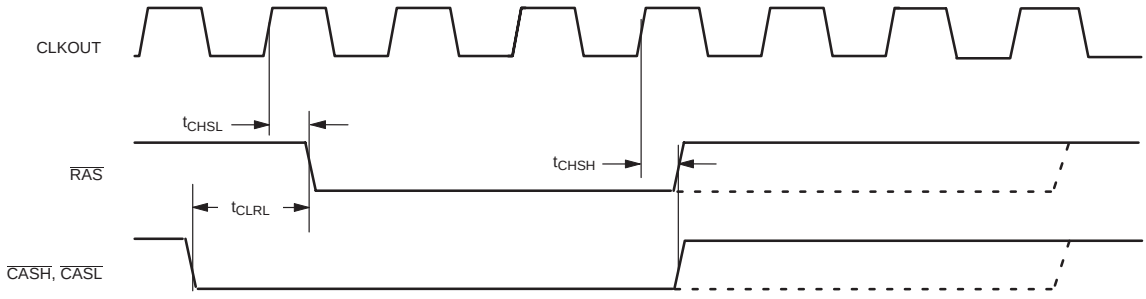


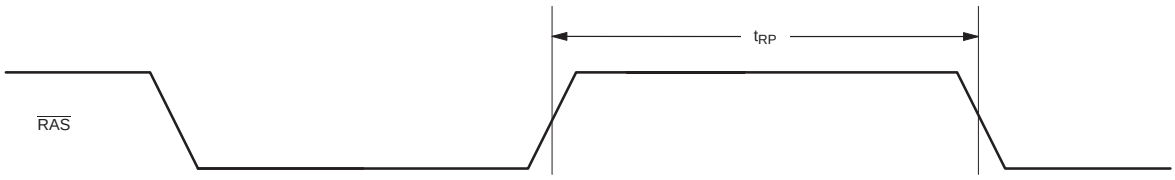
Figure 22. DRAM 16 Bit Write on 8 Bit Bus (FPM or EDO DRAMs)



$\overline{RAS}$ and $\overline{CAS}$ terminate together. The active low portion of $\overline{RAS}$ can be programmed to last from 3 to 6 clock cycles.
The high portion of $\overline{RAS}$ after Refresh can be programmed to last from 2 to 4 clock cycles. See Chapter 3 of *XA–SCC User Manual.*

SU01144

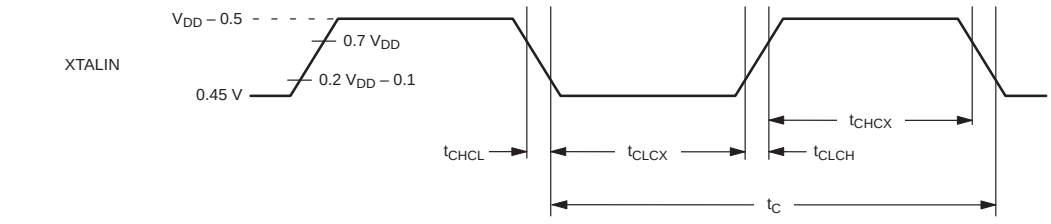
Figure 23. REFRESH



NOTE: t_{RP} min. is specified for each of the 5 individual $\overline{RAS}$ pins ($\overline{CS}\_\overline{RAS}$[5:1]).
It is the minimum high time (thus $\overline{RAS}$ inactive) between two DRAM bus cycles on the same $\overline{RAS}$ pin.

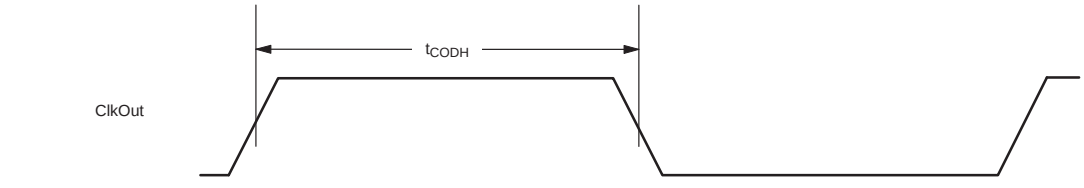
SU01145

Figure 24. RAS Precharge Time



SU01146

Figure 25. External Clock Input Drive



WARNING: ClkOut is specified into 40 pF max, do not overload.

SU01147

Figure 26. ClkOut Duty Cycle

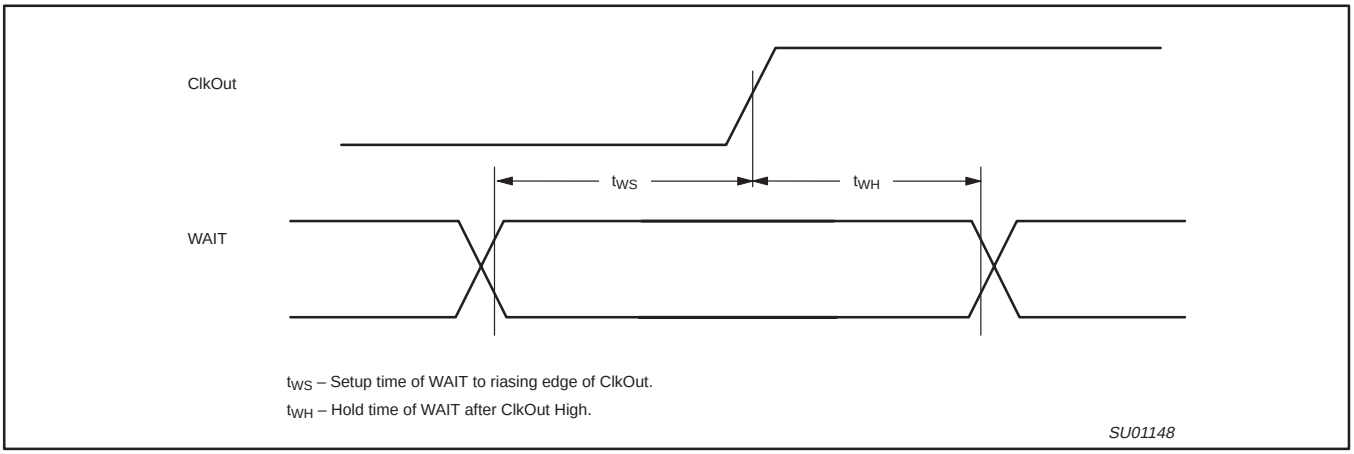
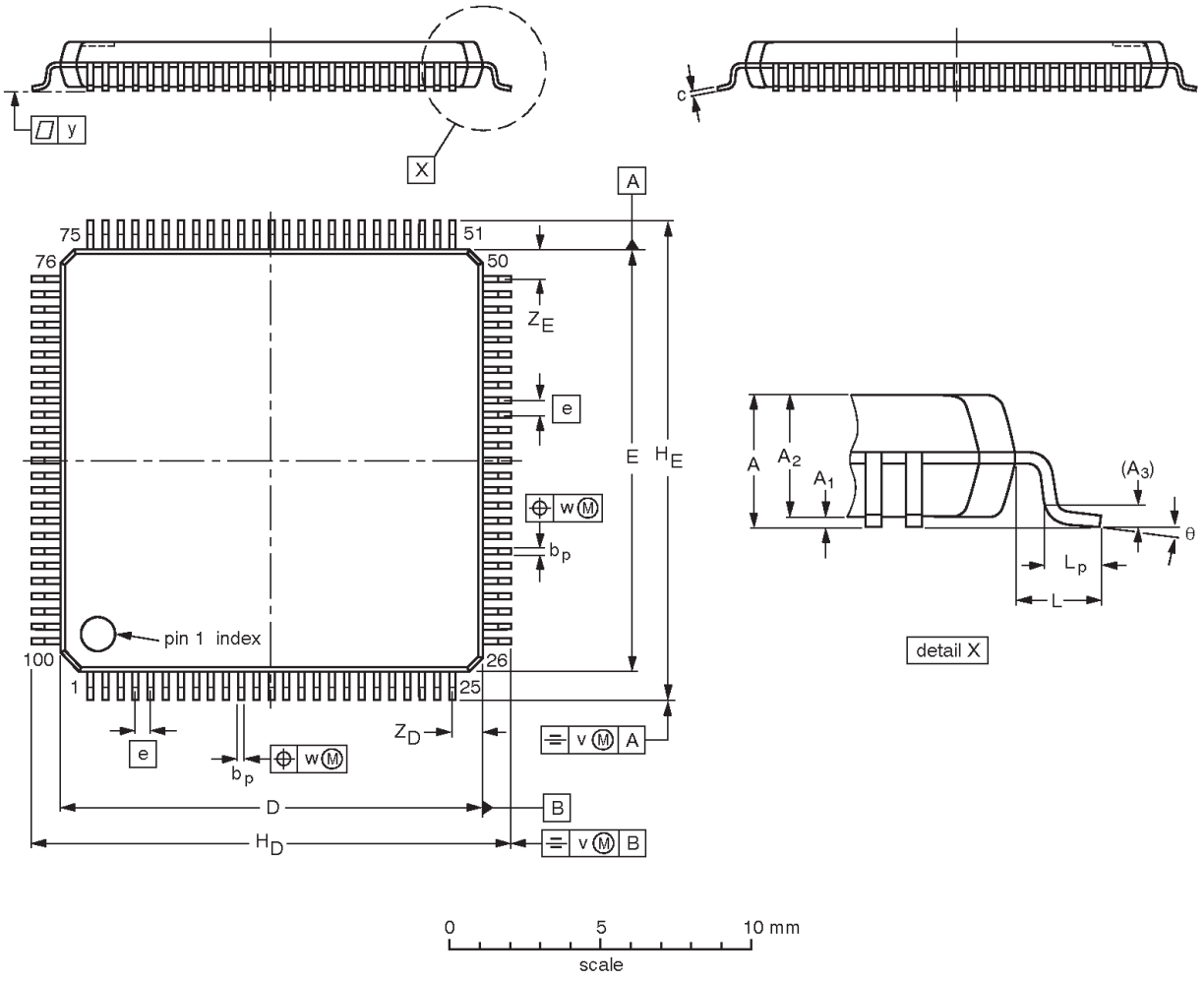


Figure 27. External WAIT Pin Timing

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						~~95-12-19~~ 97-08-04

Data sheet status

Data sheet status	Product status	Definition [1]
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Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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